TRACKING SERVOBRIDGE DETECTOR

FINAL REPORT
VOLUME I

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This report is in three volumes - Volume I describes technically the Tracking Servobridge Detector in final configuration after passing all of the requirements of MIL-D-55361(EL). Volume II describes the Production Engineering Measures required for the pilot production of these units. Volume II includes flow charts, equipment and tooling lists, sample operation sheets, other data required for production and review of the program. Volume III contains all of the Operation Sheets required to fabricate (GenRad manufactured) components and to assemble and test subassemblies and Tracking Servobridge Detectors.

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TRACKING SERVOBRIDGE DETECTOR
FINAL REPORT
VOLUME I

The object of this study is to perform the design, development engineering, fabrication of special tooling and test fixtures, obtain first article approval and establish a pilot line and pilot run for tracking servobridge detectors.

Contract No. DAAB07-73-C-0609

Prepared by:

W. J. Riley

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Section 1

ABSTRACT

1.0 General

This report is in three volumes - Volume I describes technically the Tracking Servo Bridge Detector in final configuration after passing all of the requirements of MIL-D-55361 (EL). Volume II describes the Production Engineering Measures required for the pilot production of these units. Volume II includes flow charts, equipment and tooling lists, sample operation sheets, other data required for production and review of the program. Volume III contains all of the Operation Sheets required to fabricate (GenRad manufactured) components and to assemble and test subassemblies and Tracking Servobridge Detectors.

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SECTION 3

PURPOSE

3.0 INTRODUCTION

The purpose of the Tracking Servo Bridge Detector is to facilitate accurate bridge measurements on quartz crystal resonators.

The measurement of a quartz crystal resonator is perhaps the most difficult of any passive two-terminal device. A quartz crystal displays an extremely wide range of impedance which changes very rapidly with frequency near resonance. Multiple modes must often be examined and the useful range of resonance frequencies extends across the spectrum from LF to UHF.

It is generally accepted that the most precise and accurate method to chracterize a quartz crystal resonator is in terms of equivalent-circuit parameter values determined by bridge measurements. The fact that these equivalent-circuit parameters vary widely and rapidly with frequency, however, has made bridge measurements by traditional instruments difficult, tedious and expensive. Nevertheless, accurate measurements of crystal characteristics (resonant frequency, resistance, Q, inductance, temperature coefficient, aging, etc.) are increasingly vital as frequency stability requirements become more stringent.

The advent of high quality frequency synthesizers with low phase noise and spurious levels, fine resolution and wide frequency range has made available ideal RF sources for precision bridge measurements of quartz crystals. Suitable bridges exist for manual measurements under laboratory conditions.

The Tracking Servo Bridge Detector is designed for use in conjunction with RF bridges and frequency synthesizers to measure quartz crystals with high accuracy. The unit serves as a very sensitive detector for the bridge unbalance signal, permitting measurements at power levels well below a microwatt. High detectivity (-155 dBm) is achieved by superheterodyne conversion, low-noise IF amplification and synchronous detection. The latter not only provides independent reactive and resistive unbalance detection but also permits the use of a control loop to lock the synthesizer frequency to the crystal under test, automatically maintaining reactive bridge balance. This key feature makes practical the widespread use of bridge measurements of crystals.

Other features include a X10 Frequency Multiplier (45-220 MHz) to extend synthesizers of limited frequency range, a broadband power amplifier with attenuator (+30 to -70 dBm) for control of the measurement power level, linear and log detector response modes, accurate adjustment of synchronous detector phase, a wide range of swept frequency displays for initial setup and inspection of spurious modes, and a versatile servo amplifier for locked operation and automatic lock acquisition. The frequency lock servo system not only permits fast, automatic determination of a certain characteristic frequency of the resonator (series resonance, for example) but also can follow the impedance circle to determine crystal inductance or track frequency variations versus temperature.

A frequency range of 0.8 to 220 MHz is covered. The instrument (with companion Offset LO unit) provides all needed functions for crystal measurements with a RF bridge, other than the signal source, frequency counter and oscilloscope. The accuracy of the measurement is limited only by the RF bridge.

3.1 Specification

The Tracking Servo Bridge Detector is designed to meet the requirements of MIL-D-55361 (EL). A condensed list of those specifications is presented in Table 3.1.

The single most difficult requirement is the internal RF leakage level which is below the noise level over most of the frequency range and represents a shielding factor of more than 180 dB between the RF Output and Receiver Input ports. This requirement has a profound influence on the design, from the block diagram configuration through circuit design, component selection and packaging.

Other important requirements are a low distortion broadband RF power amplifier, a low noise and wide dynamic range receiver, synchronous detectors with excellent quadrature rejection and low dc offset, and a servo integrator with exceptionally low drift.

Environmental requirements include temperature, humidity, shock vibration and altitude, all in the general context of laboratory operation. The modest temperature range of +15 to +40°C primarily effects only the dc stability of the synchronous detectors and servo integrator. The humidity requirement dictates the use of corrosion resistant metal finishes and conformal coating on the most critical electronic boards. The shock and vibration requirements influence the mechanical design of the chassis shelf and the choice of panel meters. The 10,000 foot operating altitude requirement is a factor for power supply regulator heat dissipation.

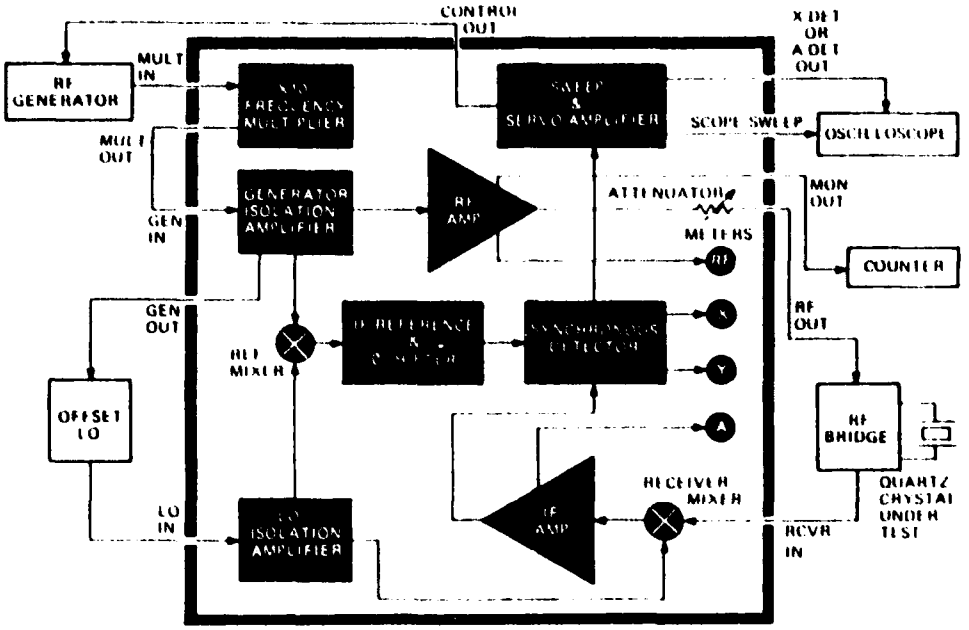


Figure 3.1. Block Diagram of Tracking Servo Bridge Detector

3.2 Block Diagram

A block diagram of the Tracking Servo Bridge Detector is shown in Fig. 3.1. The diagram shows the major functional modules (except for the power supplies) and the main signal paths between them. The descriptions which follow are divided into three major sections.

3.2.1 Generator Section

An external rf source (a frequency synthesizer) is connected either to the Generator Input or to the Multiplier Input (in which case the Multiplier Output is connected to the Generator Input). These are 50Ω interfaces at a power level of +10 dBm.

The Generator Isolation Amplifier splits the generator signal into

Table 3.1 CONDENSED SPECIFICATIONS*

Function: The Type 2995-9503 Tracking Servo Bridge Detector is used primarily for the measurement of the electrical equivalent circuit parameters of quartz crystals. The unit serves as a sensitive heterodyne detector with facilities to lock a frequency synthesizer to that point at which an rf bridge is balanced. A sweep mode is also available to display the crystal mode spectrum.

Frequency Range: 0.8 to 220 MHz for the basic instrument and 45 to 220 MHz for the X10 frequency multiplier.

Generator, LO and Multiplier Inputs: +10 dBm nominal.

Rf Output: +30 to -70 dBm nominal, 0.8 to 20 MHz; +24 to -76 dBm nominal, 20 to 220 MHz; (continuously adjustable).

Receiver Sensitivity: -155 dBm typical equivalent input noise level in bandwidth of synchronous detector meters.

Internal Leakage: Below -145 dBm equivalent input. Typically below -155 dBm up to 150 MHz.

IF Modes: Linear and log.

RF Modes: Direct and X10 frequency multiplier.

Servo Modes: Sweep, center, lock and automatic modes are provided.

Synthesizer Compatability: General Radio 1060 and 1160 series; Hewlett-Packard 5100 series.

Detectors: Magnitude and quadrature synchronous detector meters with continuously adjustable reference phase.

RF Monitor Output: 0 dBm nominal.

LO Compatability: Generator output and control/power interface compatible with Offset LO unit.

Temperature Range: +15 C to +40 C.

Power: 99 to 121 V or 198 to 242 V, 50 to 60 Hz, 40 W nominal (without external Offset LO).

Mechanical: DIMENSIONS (wxhxd), Bench 17x7x17.5 in. (435x180x445 mm); Rack 19x7x17.5 in. (483x180x445 mm). Depth includes handles.

Weight: 38 lbs (17.2 kg). Weight includes cabinet.

*See MIL-D-55361 (EL) for complete specifications.

three isolated paths, a +7 dBm level to drive the RF Power Amplifier, a -15 dBm signal which is applied to the Reference Mixer via a 20 dB pad and a 0 dBm output for the external Offset LO unit.

The RF Power Amplifier has a main output which goes, via a 101 dB step attenuator, to the RF Output port. It also has an auxiliary 0 dBm Monitor Output to drive external frequency measuring equipment. The minimum power amplifier output is +29 dBm below 20 MHz and +23 dBm above 20 MHz. It is continuously adjustable over a 1 dB range and the actual level is indicated by a panel meter.

3.2.2 Detector Section

The detector section consists of a superhetrodyne receiver and synchronous detector system which requires a local oscillator signal offset from the generator by the IF frequency of 80 kHz.

The LO Input signal is applied to the LO Isolation Amplifier which supplies isolated +7 dBm local oscillator drive to both the Receiver and Reference Mixers. The Receiver Mixer converts the Receiver Input signal into one at the 80 kHz IF frequency. The Reference Mixer does the same thing to the internal generator signal to produce a phase coherent IF reference output.

The receiver IF signal is amplified by the IF Amplifier which has both linear and log response modes. The IF Amplifier output level is displayed on the "A" panel meter.

The reference IF signal is applied to the IF Reference and Phase Shifter which supplies phase adjustable reference signals for the synchronous detectors.

The Synchronous Detectors accept the IF Amplifier output and display the magnitude of the in-phase and quadrature components on panel meters.

3.2.3 Sweep/Servo Section

The Sweep and Servo Amplifier has a variety of control and display functions. It produces a control output signal which is connected to the frequency control input of the RF generator (synthesizer) and can cause the synthesizer frequency to follow a panel control, to be swept at adjustable deviations and rates or to lock to the null point of one synchronous detector. Auxiliary outputs provide oscilloscope horizontal and vertical signals for swept displays.

SECTION 4

NARRATIVE AND DATA

4.0 DETAILED DESIGN

4.1 X10 Frequency Multiplier

4.1.1 Introduction

The Tracking Servo Bridge Detector requires two RF drive signals, one at the measurement frequency (0.8-220 MHz) and the second offset from it by the IF frequency (80 kHz). Provision is made for an external Offset Local Oscillator Unit to produce the offset frequency, in which circumstance only a single RF source is required. The requirements for this RF source are further eased by the inclusion of a X10 Frequency Multiplier which reduces to 45 MHz the upper frequency needed.

The specifications for the X10 Frequency Multiplier call for an input of 4.5-22 MHz at a power level of +10 dBm and an output of 45-220 MHz at the same power level, with all harmonics at least 25 dB down. The unit has three overlapping bands and does not degrade the signal-to-phase-noise ratio of a high-purity synthesizer source by more than 6 dB in excess of that caused by X10 frequency multiplication alone. It uses a phase-locked-oscillator multiplier (PLOM) system as shown in the block diagram Figure 4.1.1.1 and the schematic diagram of Figure 4.1.1.2.

A voltage-controlled oscillator at the output frequency is phase-locked to 10 times the input frequency by means of a decade divider within a phase-lock loop. The system blocks are described in the following sections of this report.

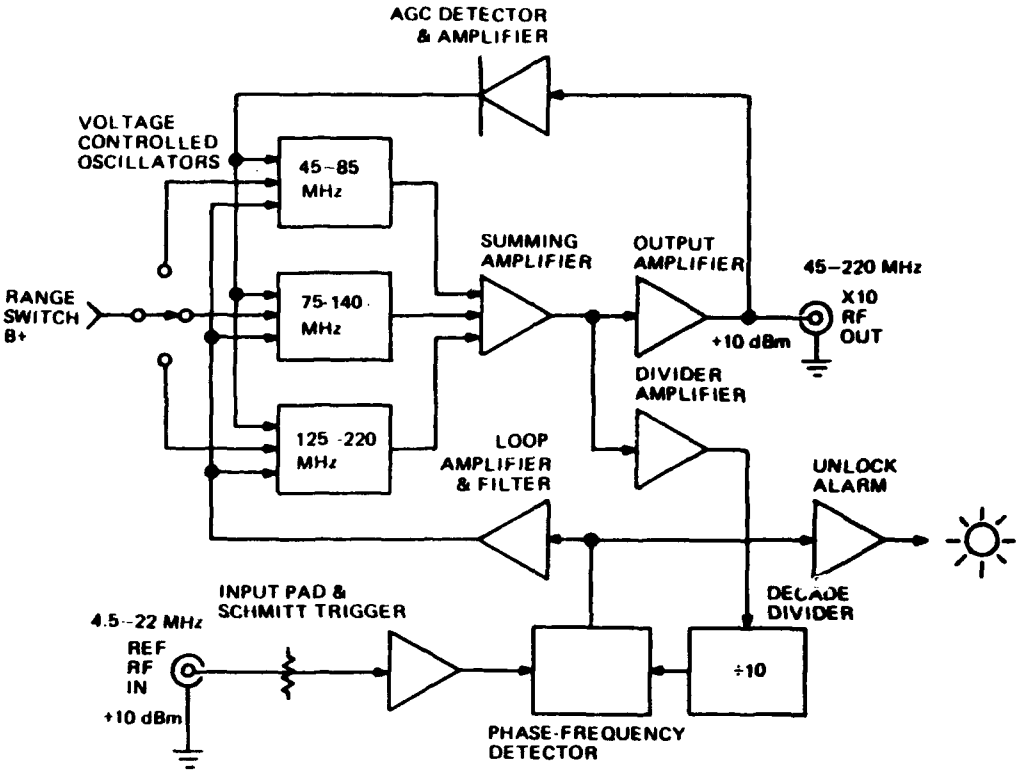


FIGURE 4.1.1.1. BLOCK DIAGRAM OF X10 FREQUENCY MULTIPLIER

4.1.2 Voltage Controlled Oscillators

The heart of the X10 Frequency Multiplier is a set of three voltage-controlled oscillators (VCO's) each having a tuning ratio of nearly 2:1. The three ranges are 45-85 MHz, 75-140 MHz, and 125-220 MHz which cover the overall 45-220 MHz range with overlaps of 10 and 15 MHz.

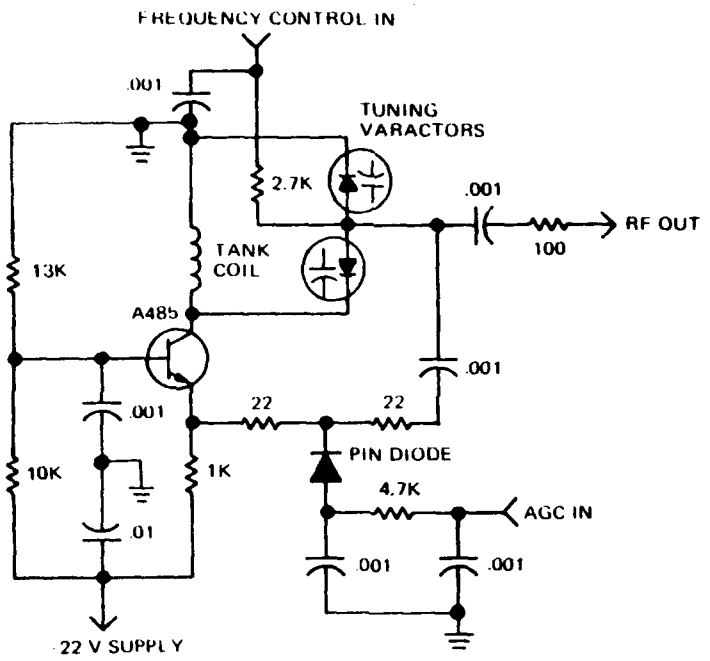
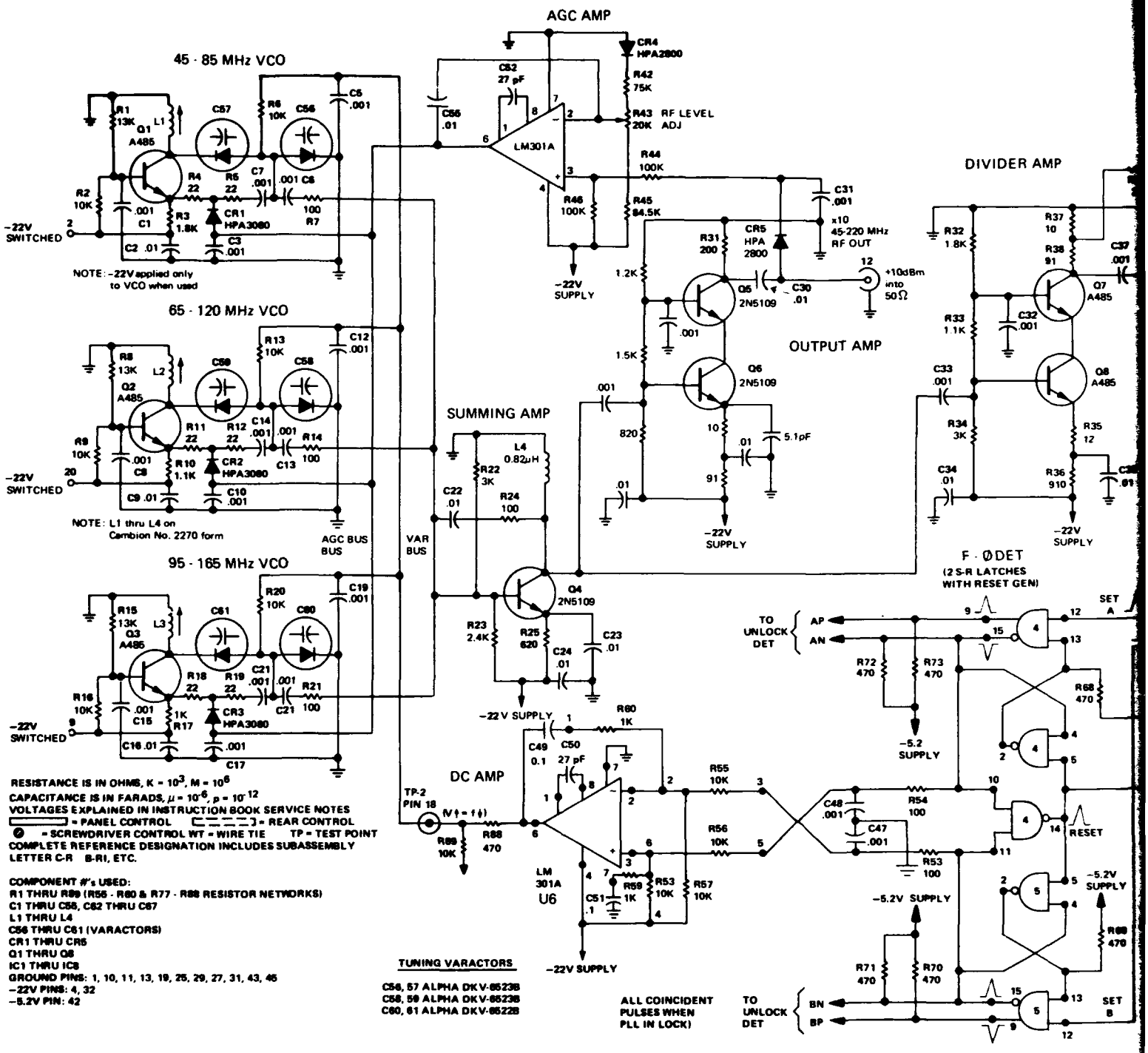


FIGURE 4.1.2. TYPICAL VOLTAGE-CONTROLLED OSCILLATOR

Figure 4.1.2 is the VCO circut diagram; the oscillator circuit is identical for each of the three ranges except for the tank coil and tuning varactors. It is a grounded-base-amplifier with positive feedback from collector to emitter. The impedance step-down in the feedback path, which is a necessary condition for oscillation, is accomplished by tapping off at the junction of the two series-connected tuning varactors. Alternate methods, such as link coupling, an inductive tap, or a separate capacitive divider, are less satisfactory. They have the disadvantages of a more complicated tank coil and trouble-



RESISTANCE IS IN OHMS, K = 10^3, M = 10^6
CAPACITANCE IS IN FARADS, $\mu = 10^{-6}$, $p = 10^{-12}$
VOLTAGES EXPLAINED IN INSTRUCTION BOOK SERVICE NOTES
▭ = PANEL CONTROL ⊏⊐⊏⊐ = REAR CONTROL
Ø = SCREWDRIVER CONTROL WT = WIRE TIE TP = TEST POINT
COMPLETE REFERENCE DESIGNATION INCLUDES SUBASSEMBLY LETTER C-R B-RI, ETC.

COMPONENT #'s USED:
R1 THRU R89 (R56 - R60 & R77 - R88 RESISTOR NETWORKS)
C1 THRU C55, C62 THRU C67
L1 THRU L4
C56 THRU C61 (VARACTORS)
CR1 THRU CR5
Q1 THRU Q8
IC1 THRU IC8
GROUND PINS: 1, 10, 11, 13, 19, 25, 29, 27, 31, 43, 45
-22V PINS: 4, 32
-5.2V PIN: 42

TUNING VARACTORS
C56, 57 ALPHA DKV-65238
C58, 59 ALPHA DKV-65238
C60, 61 ALPHA DKV-65228

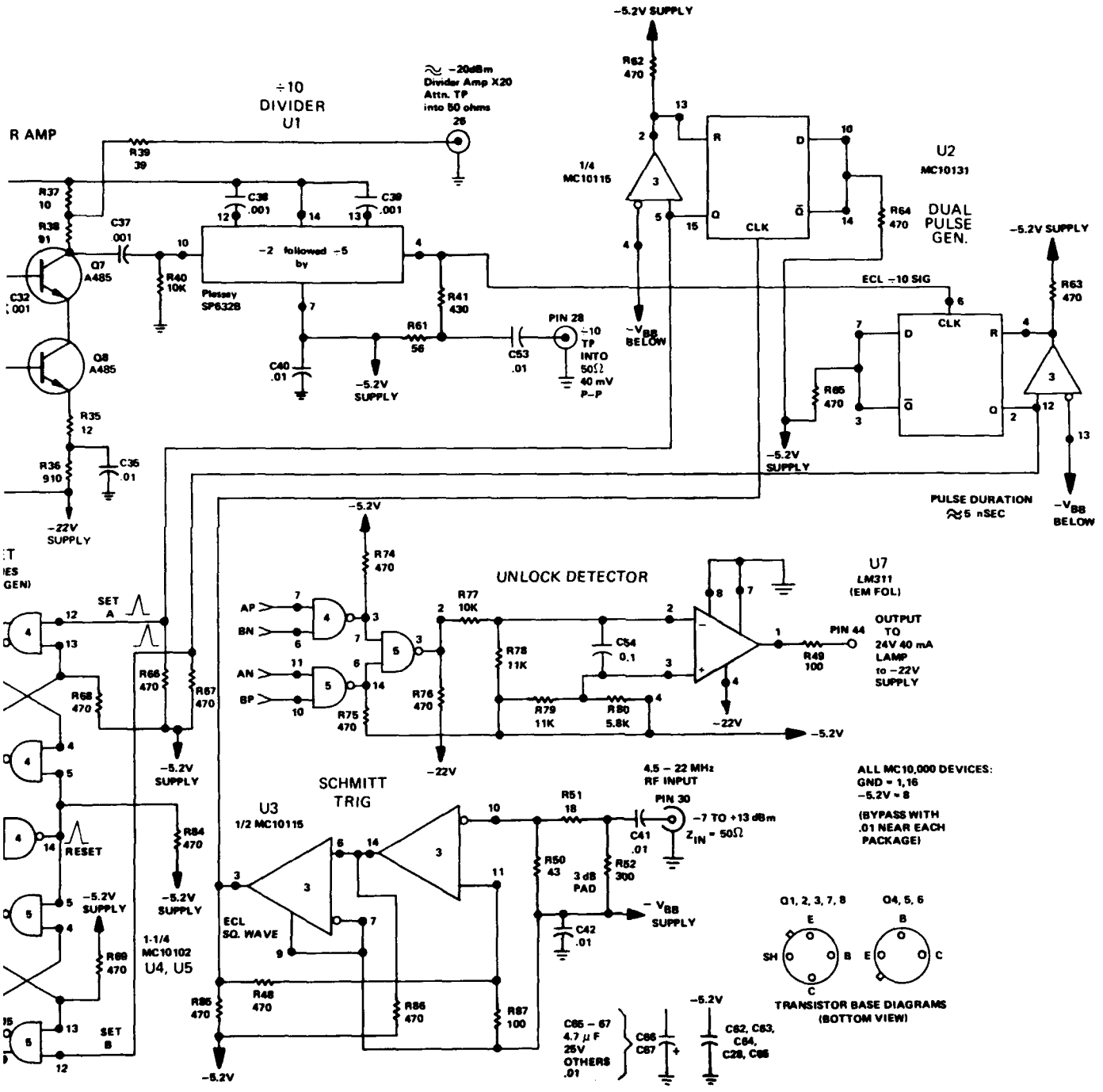


FIGURE 4.1.1.2. X10 FREQUENCY MULTIPLIER, SCHEMATIC DIAGRAM

2

some leakage reactance problems, or of additional shunt capacitance which restricts the tuning range.

If the harmonic distortion of the oscillator output signal could not be kept to about 30 dB below the fundamental level, low pass filters would have been required. A complex filter configuration would have been necessary to provide significant second harmonic attenuation over a frequency range of nearly 2:1. Low harmonic levels are obtained directly by the use of an automatic-gain-control (AGC) loop which senses the output from the X10 multiplier and varies the oscillator loop gain to prevent saturation. A PIN diode is used as a variable RF attenuator in the oscillator feedback path to accomplish this function. The PIN diode is polarized as shown to provide isolation between the AGC bus and all "off" VCO's.

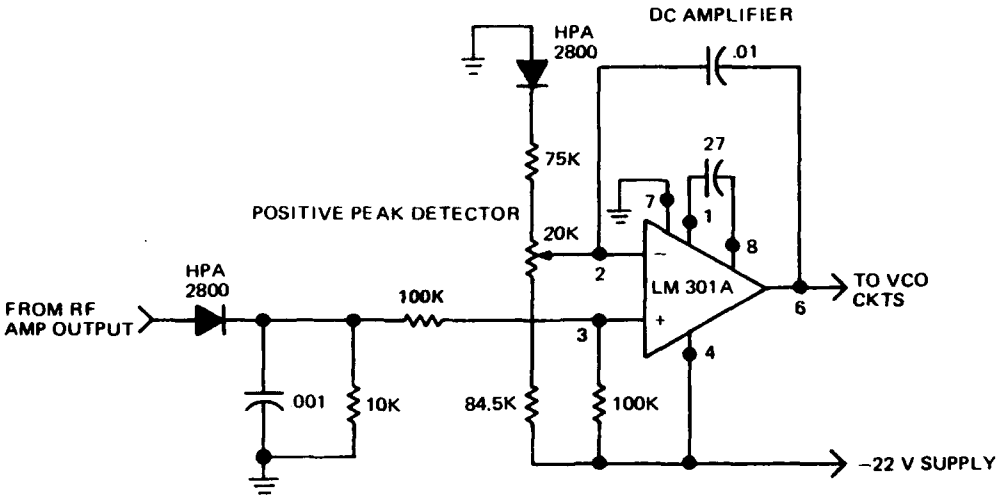


FIGURE 4.1.3. AGC DETECTOR & AMPLIFIER

4.1.3 AGC Detector & Amplifer

Automatic gain control of VCO, used primarily to reduce distortion, is performed by the circuitry shown in Figure 4.1.3.

A positive-peak detector is used to measure the +10 dBm output level. This dc voltage is compared with a reference level by an operational amplifier which in turn drives the PIN diode variable attenuator in the VCO.

4.1.4 Summing Amplifier

The outputs of the three VCO's (no two of which can be active at the same time) are combined in the summing amplifier circuit shown in Figure 4.1.4. It is a shunt feedback stage with three input resistors which operates in the same manner as the summing operational amplifier. The stage is designed to have the required frequency response (45-220 MHz) and harmonic distortion (better than 30 dB down).

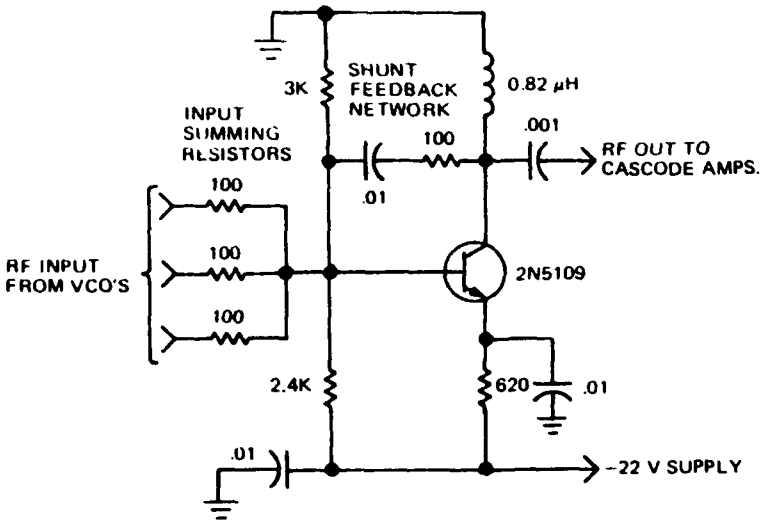


FIGURE 4.1.4. SUMMING AMPLIFIER

4.1.5 Output Amplififer

The required +10 dBm output from the X10 multiplier unit is produced by the cascode amplifier stage shown in Figure 4.1.5. Each of the two 2N5109 transistors has a power dissipation of about 250 mW, well within it's

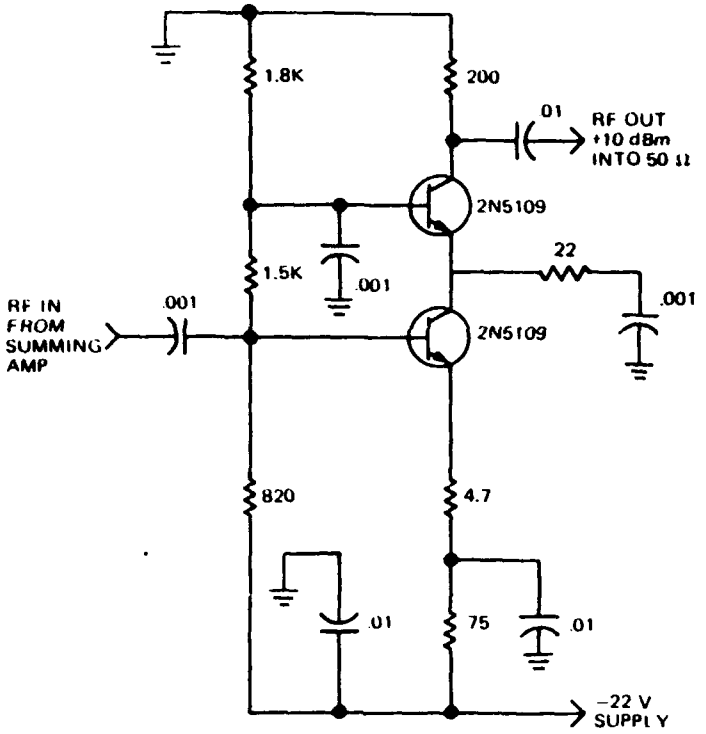


FIGURE 4.1.5. OUTPUT AMPLIFIER

75°C ambient rating of 700 mW. The summing amplifier and cascode output stage have a combined gain of 18 dB when driven from a 50Ω source matched with a 50Ω input resistor. The gain is flat to within ±1 dB over the 45-220 MHz band and all harmonics are down 35 dB or more while producing +10 dB into a 50Ω load. In the actual instrument, this output drives a power amplifier which produces the drive power for the RF bridge.

4.1.6 Divider Amplifier

The summing amplifier also drives a second cascode amplifier which provides the input for an ECL decade divider. This amplifier has sufficient isolation to keep spurious components from the digital logic down by about 60 dB in the VCO output. Details are shown in Figure 4.1.6.

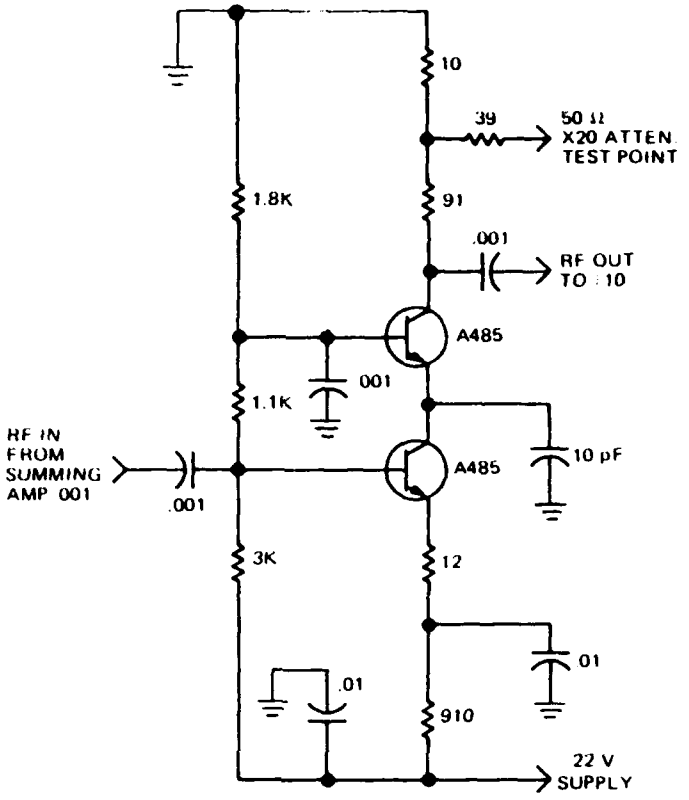


FIGURE 4.1.6. DIVIDER AMPLIFIER

4.1.7 Decade Divider

This is a straightforward application of ECL decade divider. The Plessey SP632B device used is specified for sinusoidal input signals from 40 to 400 MHz.

4.1.8 Input Schmitt Trigger

The RF reference input signal (which is to be multiplied in frequency by a factor of ten) is applied to the circuit shown in Figure 4.1.8. It consists of a 3-dB pad with 50Ω input impedance and two ECL differential amplifiers connected in series, with positive feedback. This Schmitt trigger circuit is used to convert the +10 dBm sinusoidal input into a signal having an ECL waveform.

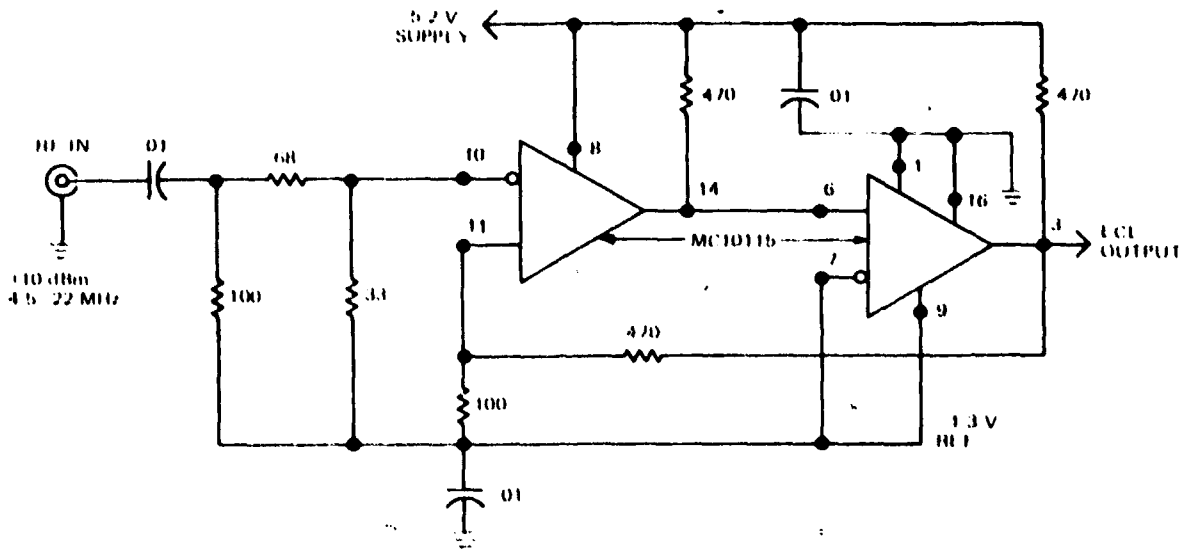


FIGURE 4.1.8. INPUT SCHMITT TRIGGER

4.1.9 Phase-Frequency Detector

It is highly desirable to augment the usual phase-detector function with a frequency-difference indication in a multiplier system of this type. This not only insures that the phase-lock loop will "capture" but also insures that lock will occur only at a VCO frequency ten times that of the reference input.

The basic phase-frequency detector logic used is shown in Figure 4.1.9.1. It consists of two set-reset latches (each implemented with two 2-input positive NAND gates) and another gate which is used as a reset generator. The operation of the circuit is as follows: The first input pulse to arrive sets its corresponding latch. The circuit will remain in this state until a pulse arrives at the other input (whether or not additional pulses arrive at the first input). The pulse at the other input first sets that latch and then the reset gate immediately resets both latches. Thus the circuit will produce the following outputs:

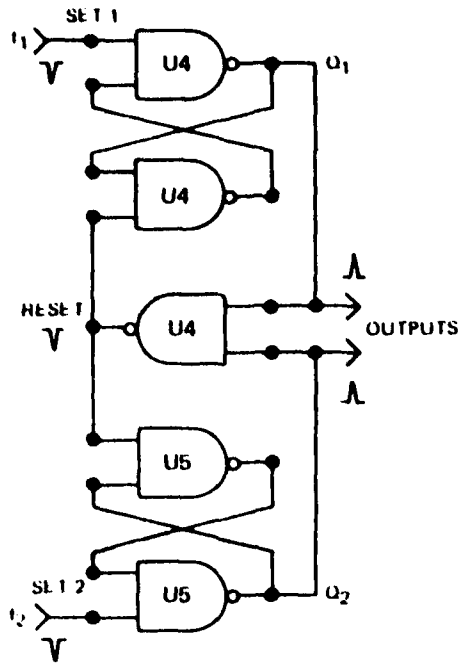


FIGURE 4.1.9.1. PHASE-FREQUENCY DETECTOR

$f_1 > f_2$ The Q_1 output will be a variable duty ratio pulse train, varying from approximately 0 to 100% at the rate $\Delta f = f_1 - f_2$. The Q_2 output will be low except for the duration of the narrow input pulse.

$f_2 > f_1$ The Q_1 and Q_2 outputs will be the reverse of that described above.

$f_1 = f_2$ One of the two outputs will be low except for the duration of the narrow input pulse.

The other output will be a certain fixed duty ratio which is dependent on the phase relation of the two input signals.

Used in a phase-lock loop with high dc gain, this phase detector will operate at a nominal 0° phase relation. Both outputs will be low except

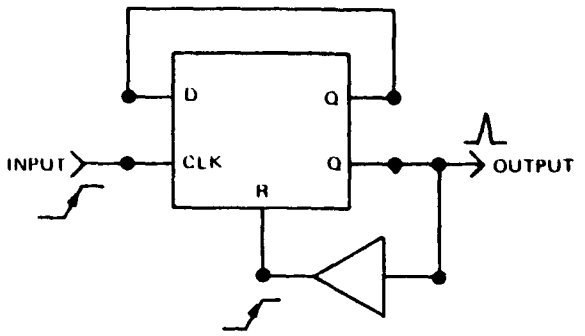


Figure 4.1.9.2 Typical Pulse Generator

for identical positive pulses during the duration of the (coincident) input pulses. The output, which is taken differentially, is the nearly-zero signal determined by the static error coefficient set by the dc loop gain. Since both outputs are identical is becomes immaterial from which direction the loop approached lock. But before lock, when $f_1 \neq f_2$, an error signal is produced which forces the loop toward the condition $f_1 = f_2$ and $\phi_1 = \phi_2$.

The phase-frequency detector also contains a pulse generator for each input as shown in figure 4.1.9.2. A D-Type flip-flop is triggered by the positive-going transition of the input signal, causing the Q output to go positive. This output, delayed by passing through a gate, is used to rest the flip-flop. The circuit thus generates a positive pulse which has a duratio equal to the propogation delay of the gate plus that of the flip-flop reset input.

4.1.10 Unlock Alarm

The phase-frequency detector produces coincident output pulses only under locked conditions. This is the operating principle of the unlock-alarm circuit shown in Figure 4.1.10.

The coincidence of the detector pulses is sensed by the exclusive-

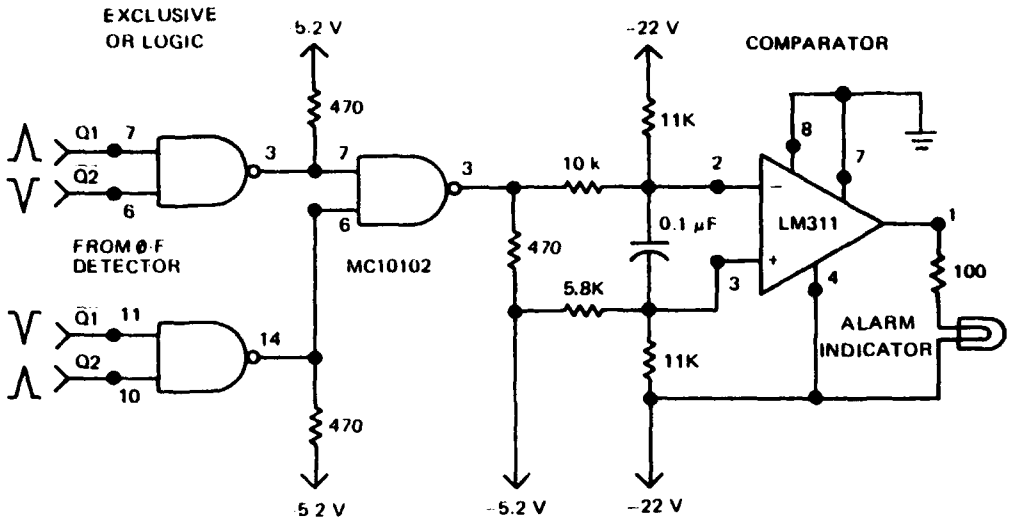


FIGURE 4.1.10. UNLOCK ALARM

or logic function which has an output that is high when the loop is locked and a variable duty ratio pulse train when the loop is unlocked. The resulting change in dc voltage is detected by a comparator which drives the unlock-alarm indicator. The unlock-alarm warns against any of the following conditions.

1. No reference signal.
2. No oscillator signal.
3. Reference signal outside lock range of oscillator.
4. AC on lock loop for any reason.
5. Failure of the Summing Amplifier, Divider Amplifier, Decade Divider, Pulse Generators, or Input Schmitt Trigger.
6. Loss of -5.2 V supply.
7. Most failures of Phase-Frequency Detector.

Loss of the -22 V supply, while not indicated by the alarm, will result in no output from the multiplier, thus no wrong output. The alarm circuit itself can be checked by simply removing the reference signal and observing that the alarm indiator illuminates.

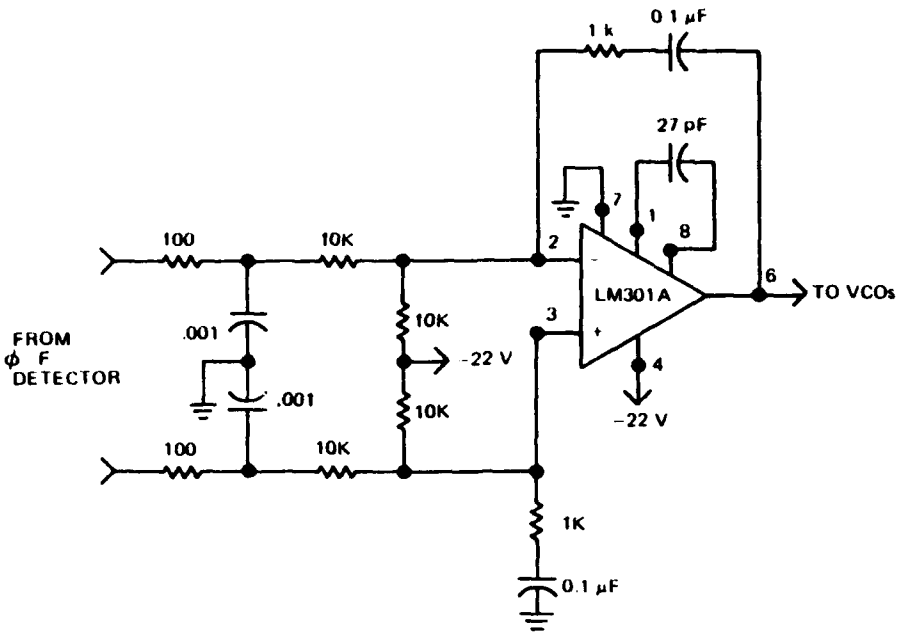


FIGURE 4.1.11.1. DC AMPLIFIER & LOOP FILTER

4.1.11 Phase-Lock Loop DC Amplifier & Compensation Network

The phase-frequency detector produces two output signals which are used as the inputs to a differential amplifier that closes the overall phase-lock loop. Several passive networks ahead of, and associated with, the operational amplifier, shown in Figure 4.1.11.1, serve to shape the frequency response of the loop and thus ensure a stable servo-system.

Detailed analysis of phase-lock loop behavior has appeard in the technical literature numerous times and will not be repeated here. The basic open-loop response G, in the absence of any filters or other low pass breaks, is given by:

$$G = \frac{\omega_c}{s}$$

where $$\omega_c = \frac{K_\phi K_a K_v}{N} \text{ rad/sec}$$

and K_{ϕ} = phase detector sensitivity in volts/radian

K_a = amplifier gain in volts/volt

K_v = VCO tuning sensitivity in rad/sec per volt

N = Divider factor (10)

For a flat amplifier characteristic, the open-loop response is that of an ideal integrator, the result of the VCO block. Phase, the loop variable under consideration, is the integral of the VCO frequency. Unity open loop gain occurs at radian frequency ω_c.

The Tracking Servo Bridge Detector has an IF bandwidth of 2 kHz so it is desirable to have substantial loop gain up to this frequency to reduce the noise contribution of the VCO and maintain a tight lock to the stable reference signal. Servo stability considerations demand a nominal -6dB/octave rolloff in the region where the open-loop gain becomes unity, but it is desirable to increase the gain more rapidly in the region below ω_c for improved VCO noise reduction.

The loop is therefore stabilized by means of a compensation network which rolls off the gain more rapidly in the region below about 2 kHz and then returns to a -6 dB/octave rolloff in the region where the open-loop gain becomes unity, now reduced to about 20 kHz. This shaping is done by the series RC feedback networks in conjunction with the source impedance. Additional networks provide high frequency filtering and dc translation.

The resulting open-loop response of the overall phase-lock loop is shown in Figure 4.1.11.2. Curves are shown for both minimum and maximum gain, a function of RF frequency and of the VCO in use. Although potentially unstable

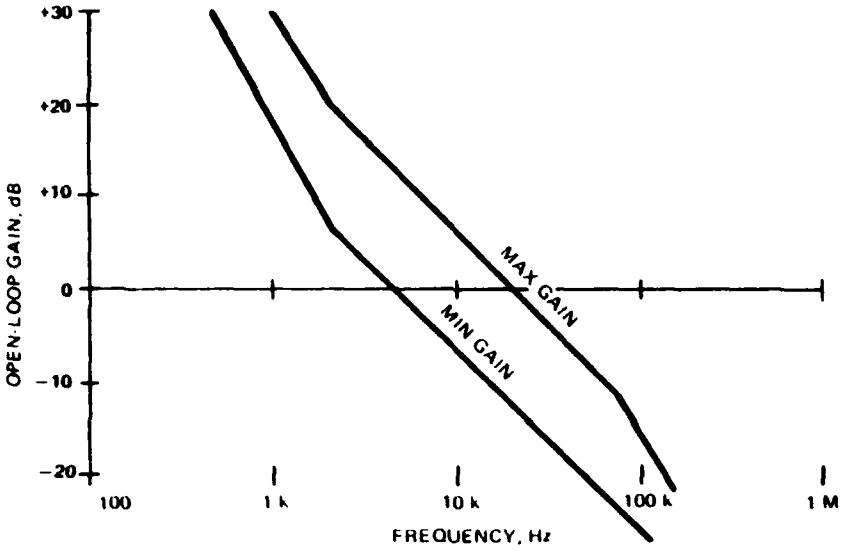


FIGURE 4.1.11.2. OPEN-LOOP RESPONSE OF PHASE-LOCK LOOP

for conditions of both low and high gain, the system has a margin in either direction. The loop provides at least 20 dB of negative feedback for VCO phase noise at sideband frequencies of 1 kHz and below.

4.1.12 Test & Performance Data

The performance of the X10 Frequency Multiplier has been found very satisfactory. The following test results are typical:

Frequency Range (Specification: see nominal range values)

Nominal Range MHz	Actual Range MHz
45 - 85	38 - 95
75 - 140	62 - 157
125 - 220	108 - 244

RF Output (Specification: +10 dBm nominal)

+9.5 dBm ±0.5 dB

Harmonic Distortion (Specification: -25 dB)

Better than 30 dB down (except for a X2 peak of about -25 dB around 400 MHz which is far outside the power amplifier passband).

Divider Spurious Components (Specification: none)

Typically - 55 dB

Largest - 48 dB

Input Level (Specification: +10 dBm nominal)

Locks with input signal below -7 dBm

Power Consumption (Specification: none)

-22V @ 100 mA = 2.2 W

-5.2V @ 300 mA = 1.6 W

Total 3.8 W

Input Impedance (Specification: 50Ω nominal)

Established by a 50Ω resistive input pad.

Phase Noise (Specification: less than 17 mrad. rms in 30 kHz bandwidth excluding ±3 Hz from carrier)

5-10 mrad rms

4.2 Power Supply

4.2.1 General

This instrument has two entirely separate ac line power supplies. One, the Main Preregulator, supplies ±18V to most of the instrument modules. These modules are each provided with on-board ±15V integrated circuit voltage regulators. The other supply produces -22V and -5.2V for the RF module.

Provision is made to supply power to the external Offset LO Unit.

The characteristics of these two power supplies are shown in Table 4.2.1.

4.2.2 Main Preregulator

Two integrated circuit three-terminal regulators are used for this circuit since the regulation requirements for the +18V Main Preregulator are very modest. The circuit diagram is shown in Figure 4.2.1.

The IC regulators each are 15V units which are used to provide an adjustable 18V output by a resistive divider in the ground lead. Overload protection is provided by built-in current limiting with thermal shutdown.

4.2.3 RF Module Supply

The RF Module supply has more stringent requirements (in particular, a need for the outputs to track). The circuit diagram is shown in Figure 4.2.2.

This circuit uses IC op-amps, monolithic power Darlington transistors and a single stable reference Zener diode.

The basic (positive) regulator circuit is shown in Figure 4.2.3.

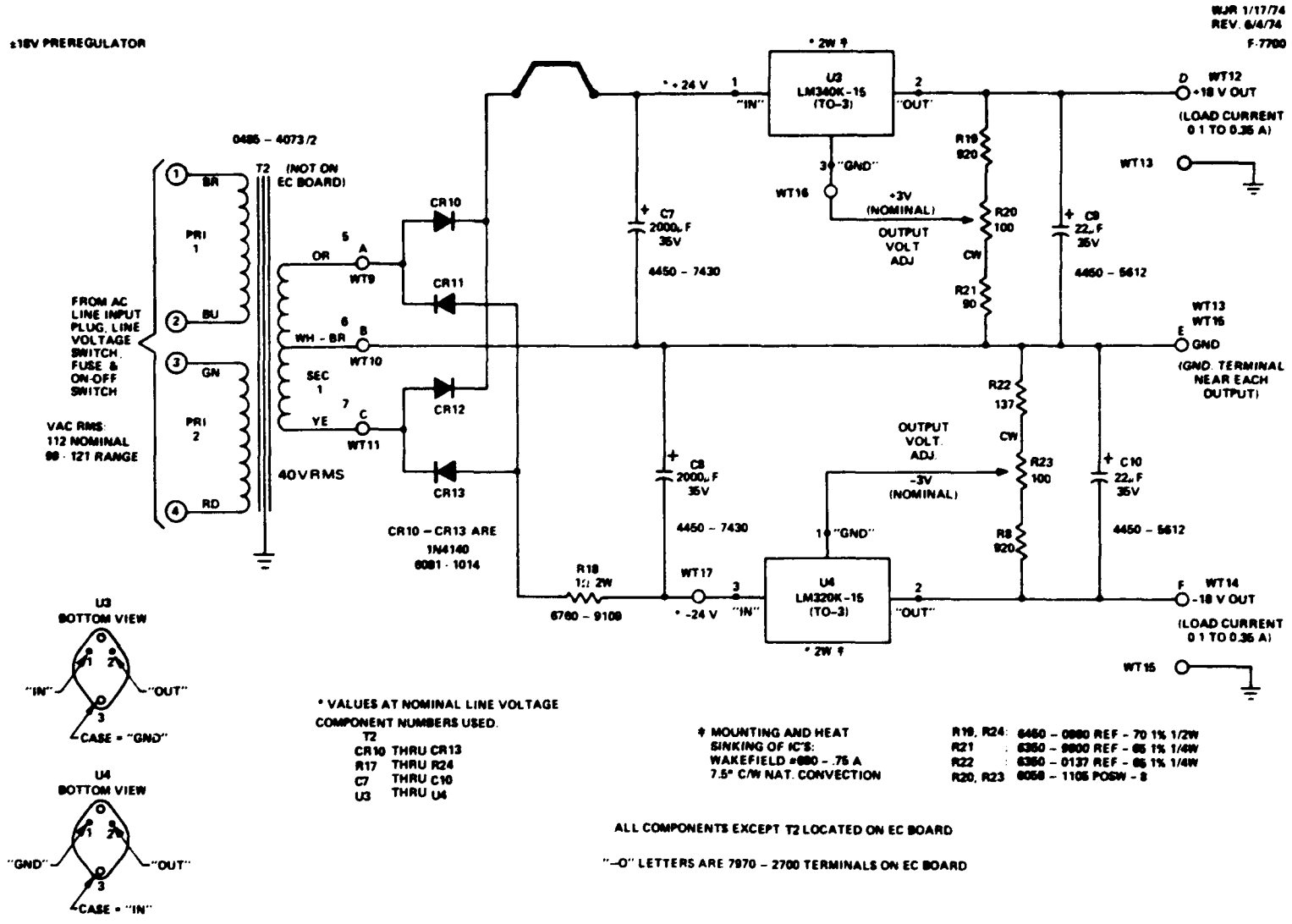


FIGURE 4.2.1. MAIN POWER SUPPLY, SCHEMATIC DIAGRAM

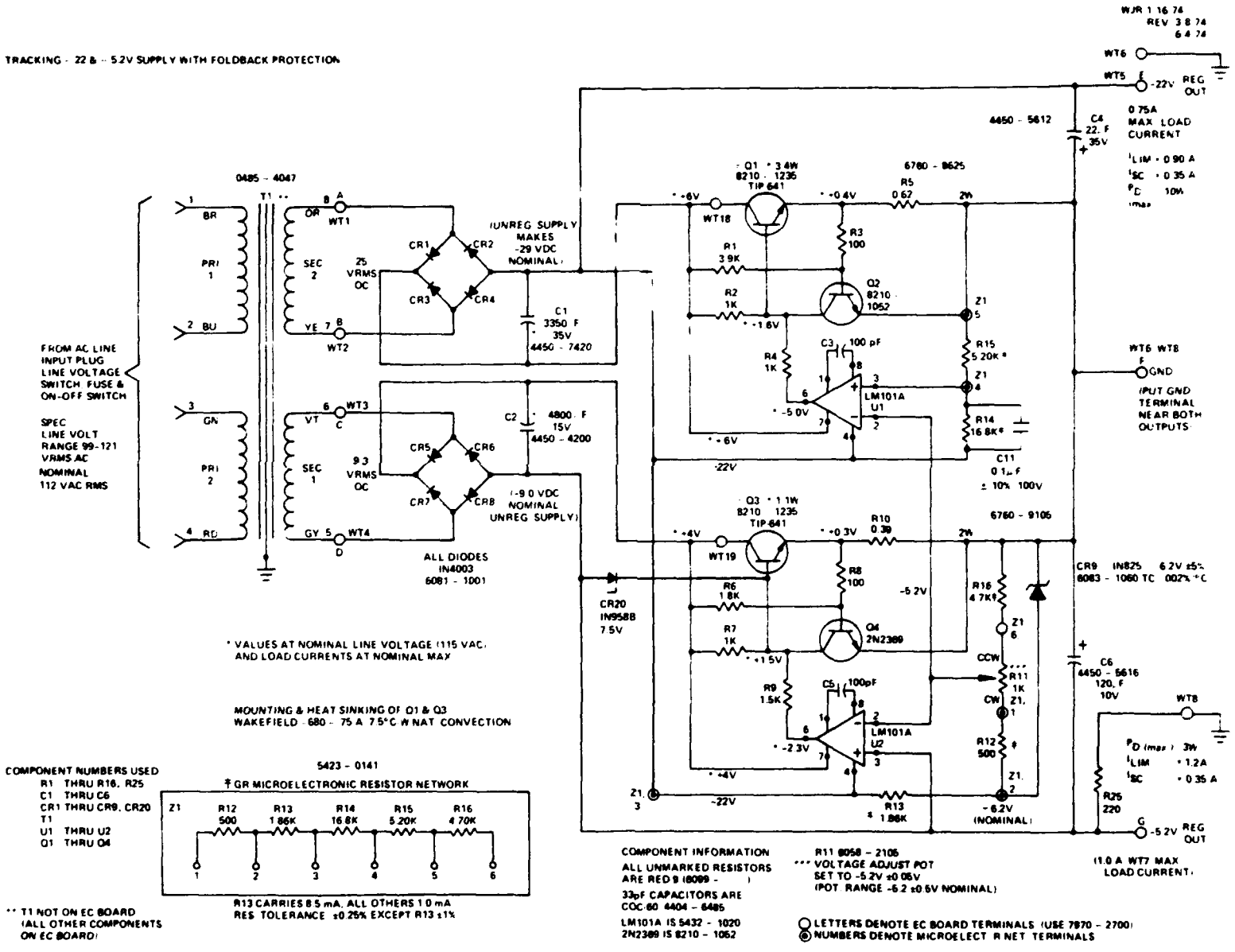


FIGURE 4.2.2. RF MODULE POWER SUPPLY, SCHEMATIC DIAGRAM

Table 4.2.1

Power Supply Characteristics

Power Supply	Output Voltage VDC	Load Current A	Load Power W	Voltage Stability %	Overload Protection	Notes
Main Pre-Regulator	+18	0.1-0.35	1.8-6.3	2	Current limiting with thermal shut down	0.25 a load current is allowed for external Offset LO from each output
	-18	0.1-0.35	1.8-6.3	2		
RF Module	-22	0.6-0.75	13.2 16.5	0.5	Current limiting with foldback	-22 and -5.2V outputs are tracking. Allowance is made for external Offset LO: 0.15A @ -22V 0.70A @ -5.2V
	-5.2	0.3-1.0	1.6-5.2	0.5		
		TOTAL	18.6-34.3			

AC Line Input: 99-121 VAC or 198-242 VAC,
50-60 Hz, 40W nominal
without external Offset LO

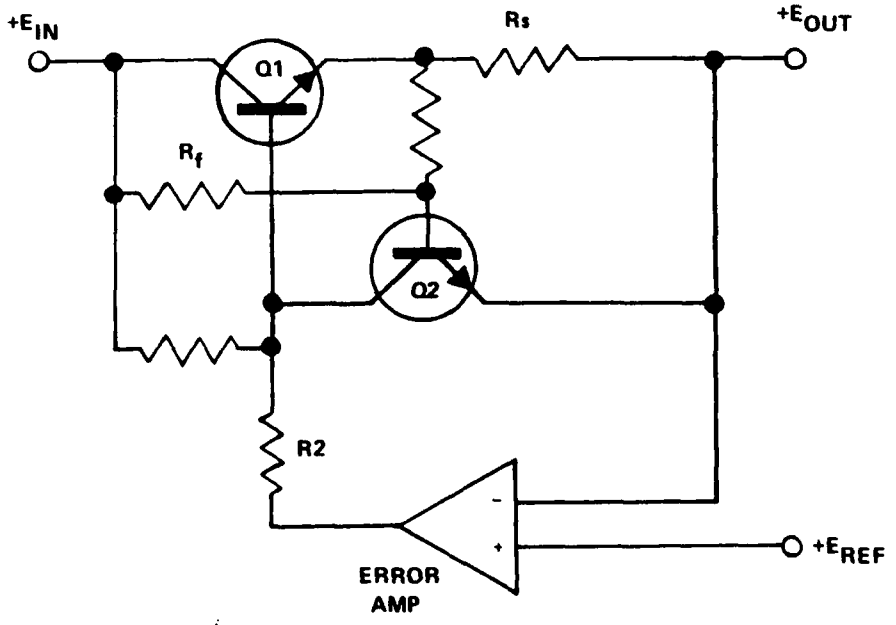


FIGURE 4.2.3. BASIC REGULATOR CIRCUIT, SCHEMATIC DIAGRAM

The circuit as shown is a power voltage follower with $E_{out} = E_{ref}$ as determined by the differential error amplifier. Series pass transistor Q1 is a power Darlington unit. Feedback stability is insured by unity gain compensation of the error amplifier itself. Overload protection is provided by current sensing resistor R_s and drive bypassing through Q2. Resistor R_f provides current foldback to reduce overload dissipation in Q1.

The actual circuit uses this configuration in the return lead of each negative supply. A single Zener diode produces a -5.2V reference voltage for each regulator. A microelectronic resistor network is used in the reference divider circuits.

4.3 RF Power Amplifer

4.3.1 General

A broadband power amplifier is required to provide the RF Output signal with low distortion and a level of at least +29 dBm from 0.8 to 20 MHz and at least +24 dBm from 20 to 220 MHz. The unit developed meets the electrical requirements,is small (5 x 2-1/2 x 1-1/8 inches), and needs no forced air cooling. The DC input is less than 10W and heat is dissipated by conduction through the case.

The basic circuit is shown in Figure 4.3.1. The output stage is a push-pull transformer-coupled circuit. The lower level stages are RC coupled. While leveling is not necessary to attain the required frequency response, the distortion of the amplifier was found to increase very rapidly with overdrive. An automatic level control was added and it ensures very low distortion levels for a $\pm$3 dB range of input drive levels. The unusally high efficiency of this design is basically due to the transformer coupling of the output stage and to

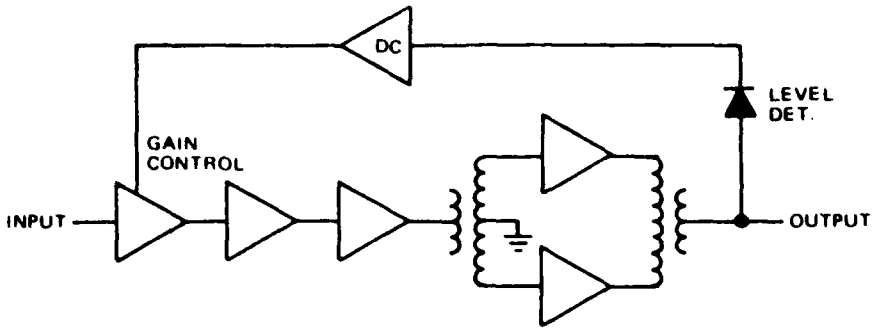


FIGURE 4.3.1. BLOCK DIAGRAM OF POWER AMPLIFIER

careful design of the circuits for excellent output matching without internal power-consuming terminations.

4.3.2 Output Stage

The most difficult part of the power amplifier is the output stage. The combination of wide bandwidth and low distortion requires transistors capable of high current and very high bandwidth. There are not many types available and economy dictates best use of the power capabilities; about 1-1/2 watts of RF output is required from the output transistors. It was decided to use a pair of NEC 1594 transistors. They are in a strip-line package with an insulated stud and are rated for 5 watts dissipation at 75°C stud temperature. It would have been possible to use the two transistors in parallel and get favorable matching conditions at the output, but the push-pull transformer-coupled configuration was chosen for its lower even-order harmonics and best use of the voltage and current capabilities of the transistors. The output transformer is a 200Ω -balanced-to-50Ω -unbalanced transmission-line variety (Z-Match, Model HF 122). The output required is about 7V rms. At the secondary of the transformer, almost 10V rms is required because of the series isolation resistor, detector loading and other losses. The primary voltage is about 20V rms. An 18V DC supply was found adequate but about 3V more is used to stabilize the operating point; the power supply requirements were established

as -22V. The transistors are biased for lowest distortion at the required power level. Each transistor has a dc current of 140 mA, and 19V between collector and emitter, for a dissipation of about 2.7W, well within the rated 5W at 75°C stud temperature.

The output transistors are driven from a 50Ω-unbalanced-to-50Ω-balanced transmission-line transformer. The transformer is an Anzac TP101.

The output matching takes advantage of the characteristics of the transformer and frequency-dependent negative feedback so that little power is wasted in internal resistive terminations. Adjustments are provided for setting and balancing the operating current in the output stage transistors.

4.3.3 Driver Stage

A single-ended class A amplifier in grounded-emitter configuration provides drive for the output stage. Negative feedback shapes frequency response and impedances. The transistor is a NEC 2SC1251 strip-line package with insulated stud. The dissipation in this stage is about 0.9W; the transistor is rated 2W at 75°C stud temperature.

4.3.4 Input Stage

This stage uses a 2N5109 in a class A, grounded-emitter amplifier configuration. Negative feedback is used to shape frequency response and impedances. The dissipation is about 0.35 watt. A small radiator (Thermalloy 2226) holds the case temperature to less than 75°C (at max specified ambient); the transistor is rated at 2.5W under these conditions.

4.3.5 Gain-Control Stage

Gain control over a modest range (+3 dB) is provided by the

basic arrangement shown in Figure 4.3.5. The grounded-base transistor is driven from the input through R1, chosen to ensure good input matching. The variable resistor R changes the gain; a PIN diode provides electronically variable gain. A diode with long lifetime keeps distortion low at the lowest frequency (0.8 MHz). The transistor is a 2N5109 with about 0.3W dissipation. A Thermalloy 2226 radiator holds the case temperature to less than 75°C at max. ambient.

4.3.6 Shaped Level Control (SLC)

An automatic-level-control circuit prevents departures from proper input level and resultant high distortion. Since the output specifications call for +29 dBm minimum to 20 MHz and +24 dBm minimum above 20 MHz, the level control must be shaped. Figure 4.3.6.1 shows the response and Figure 4.3.6.2 shows the response-shaped RF detector and the basic arrangement of the control

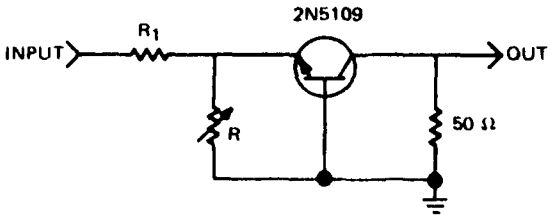


FIGURE 4.3.5. GAIN CONTROL STAGE

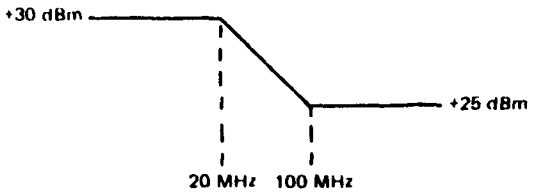


FIGURE 4.3.6.1. RESPONSE OF SHAPED LEVEL CONTROL

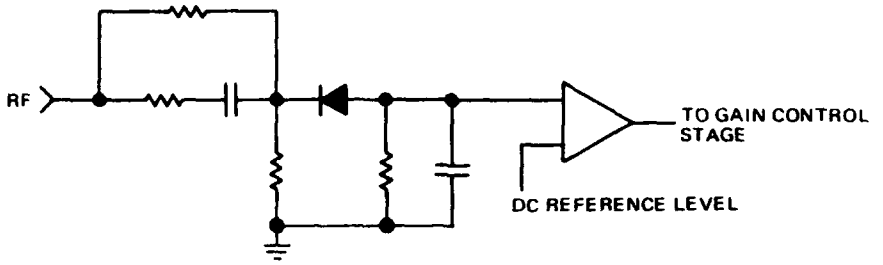


FIGURE 4.3.6.2. SLC CIRCUIT

loop. A portion of the RF output is rectified and the dc from it is compared to a dc reference voltage. Any error between the two is used to vary the gain in the gain-control stage.

4.3.7 Output Power Monitor

This circuit, located on the sweep/servo board, not only indicates output power level but proper drive level as well. Under normal drive and load conditions, the meter reads the output power, calibrated from +24 to +30 dBm, but if the drive is too low the meter is deflected below zero (down scale) and for too high a drive level, beyond full scale. The circuitry for the meter drive is discussed in Sec. 4.5.7.

4.3.8 Test and Performance Data

The performance of the RF Power Amplifier has been found to be satisfactory in all respects. Figure 4.3.8.1 shows power and VSWR vs frequency for a typical amplifier, measured at its output connector, and does not include the attenuator. Smith charts of the output impedance vs frequency are shown in Figures 4.3.8.2 and 4.3.8.3. This impedance was measured at the front panel connector and includes the effects of the line between the panel and the attentuator, the attenuator set for 0 dB (min. attenuation), and the line between attenuator and power amplifier proper. The first chart covers the frequency range from 0.5 MHz to 85MHz and the second from 85 to 260 MHz. The

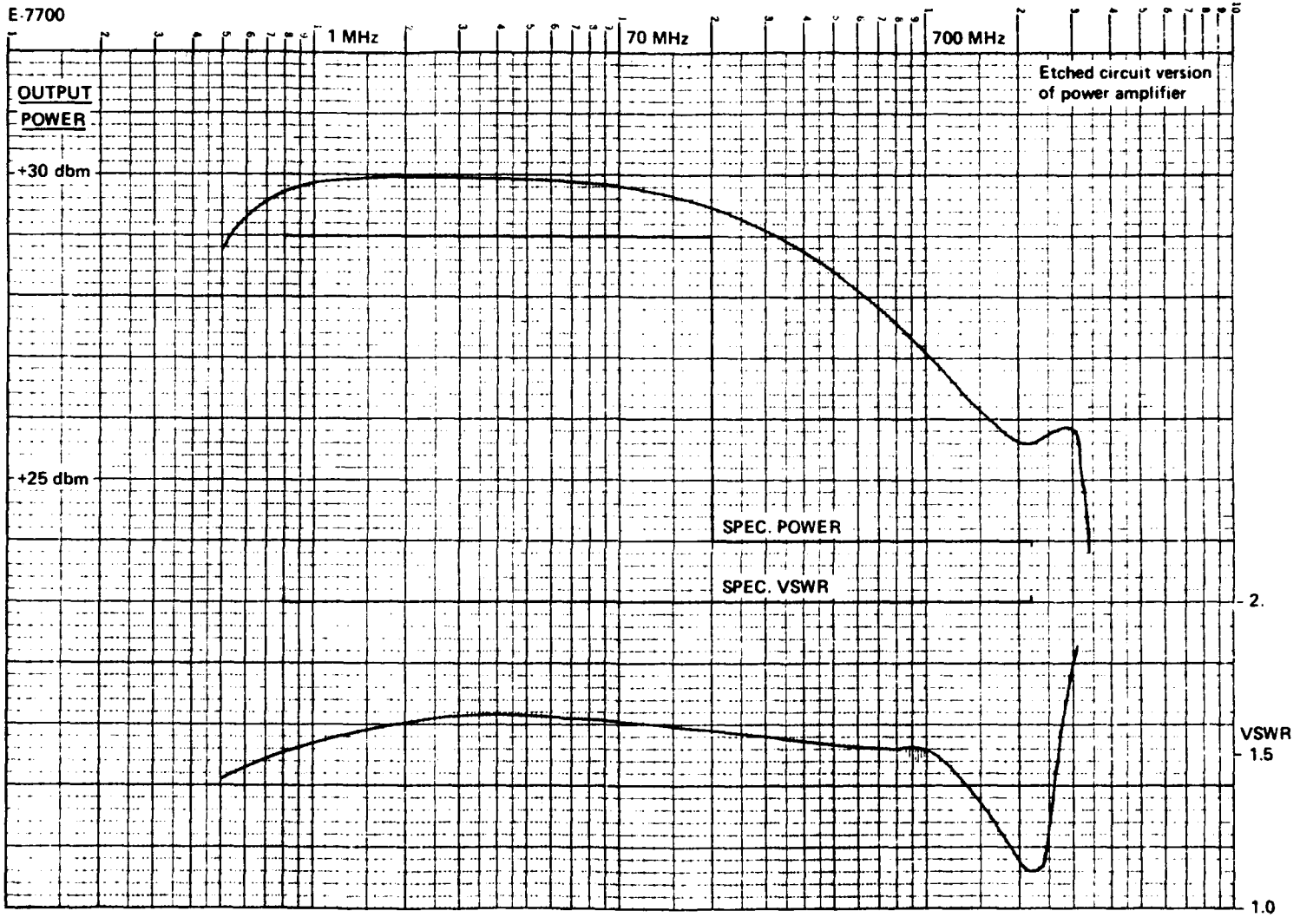


FIGURE 4.3.8.1. POWER AMPLIFIER, OUTPUT AND VSWR VS. FREQUENCY PLOT

IMPEDANCE COORDINATES—50-OHM CHARACTERISTIC IMPEDANCE

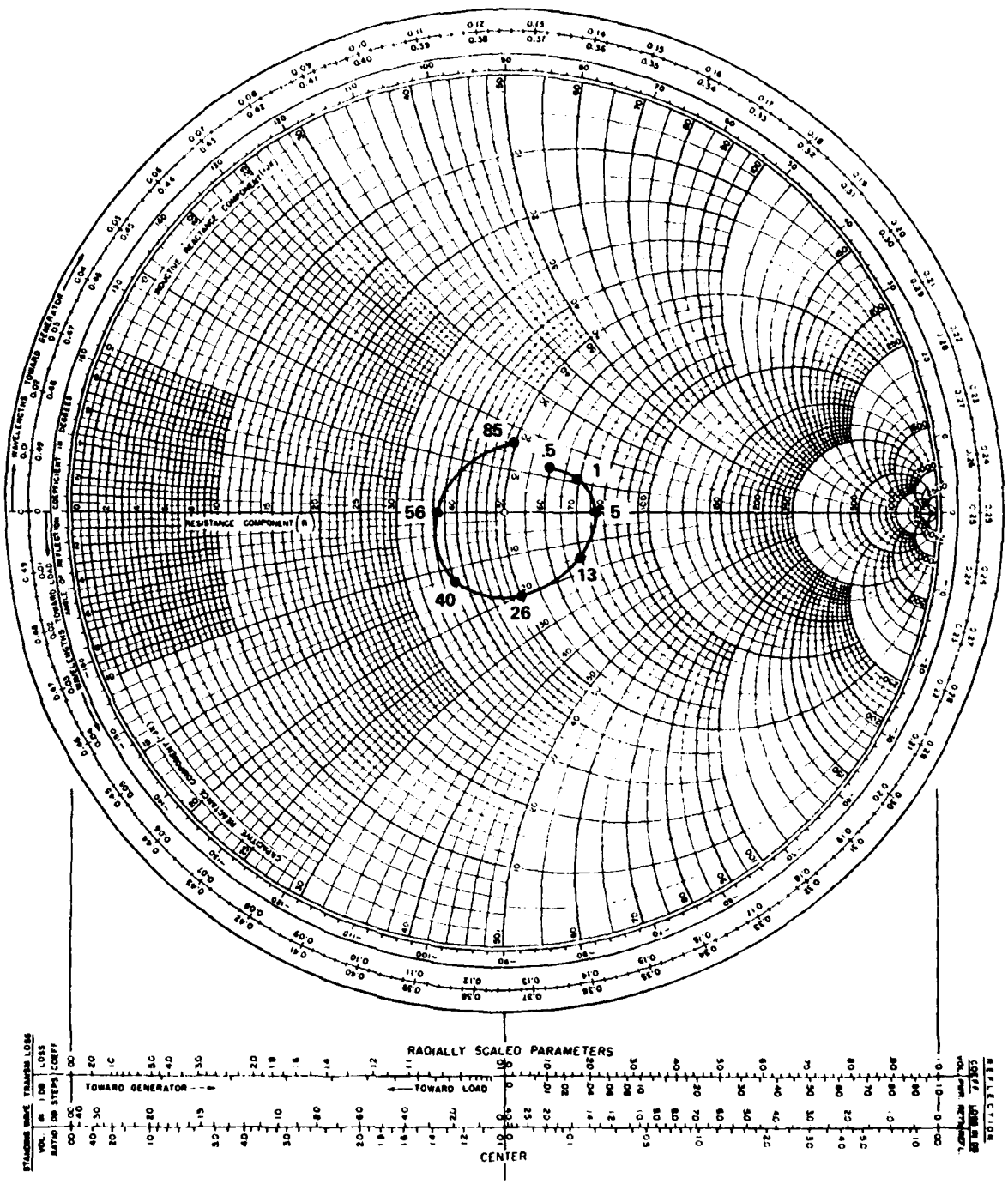


FIGURE 4.3.8.2. POWER AMPLIFIER, OUTPUT IMPEDANCE VS. FREQUENCY PLOT, 0.5 TO 85 MHz

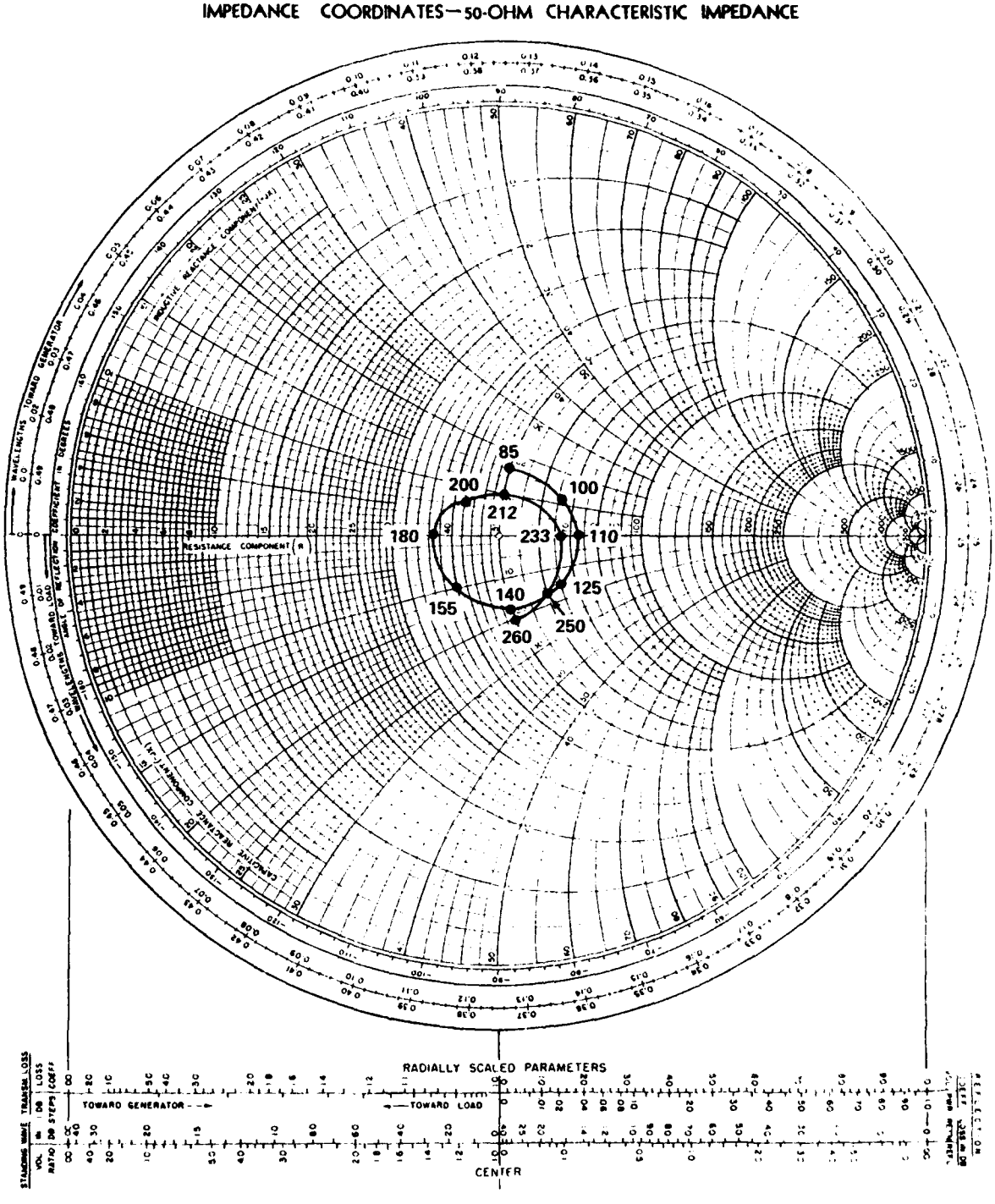


FIGURE 4.3.8.3. POWER AMPLIFIER, OUTPUT IMPEDANCE VS. FREQUENCY PLOT, 85 TO 260 MHz

harmonic distortion of the amplifier at the nominal output is less than -30 dB at all frequencies as shown in Figure 4.3.8.4. Typical input level limits are shown in Figure 4.3.8.5. The amplifier is stable for any load condition from short circuit to open circuit, but under open circuit conditions the output level exceeds the ALC limits and the meter will be off scale. The attenuator can provide the necessary minimum load, and a bridge such as the GR 1606 is satisfactory as well. The mechanical and thermal characteristics are satisfactory. When the amplifier housing is heat-sinked to the front panel of the instrument, the temperature rise at the power transistor studs is less than $10^{o}C$. Figure 4.3.8.6 shows no significant dependence of RF power output vs ambient temperature.

4.4 IF Amplifier

4.4.1 General

The primary function of the IF Amplifier in this instrument is to provide most of the gain necessary to detect the 80 kHz output from the receiver mixer. This signal can be as small as 0.5 μV rms (with -120 dBm at mixer signal port). Under conditions of extreme bridge unbalance, however, large IF input signals levels (greater than 1V rms) may occur. When swept-frequency measurements are being made, the signal level may change rapidly.

4.4.2 Design Considerations

To provide satisfactory performance under these varied conditions the IF amplifier must have both linear (manual gain control) and log modes. In the manual gain control (MGC) mode the gain is variable from 0 to +120 dB. The log mode small-signal gain can be preset at any value between +70 and +100 dB. Both modes provide low noise at high gain and handle large signals at low gain.

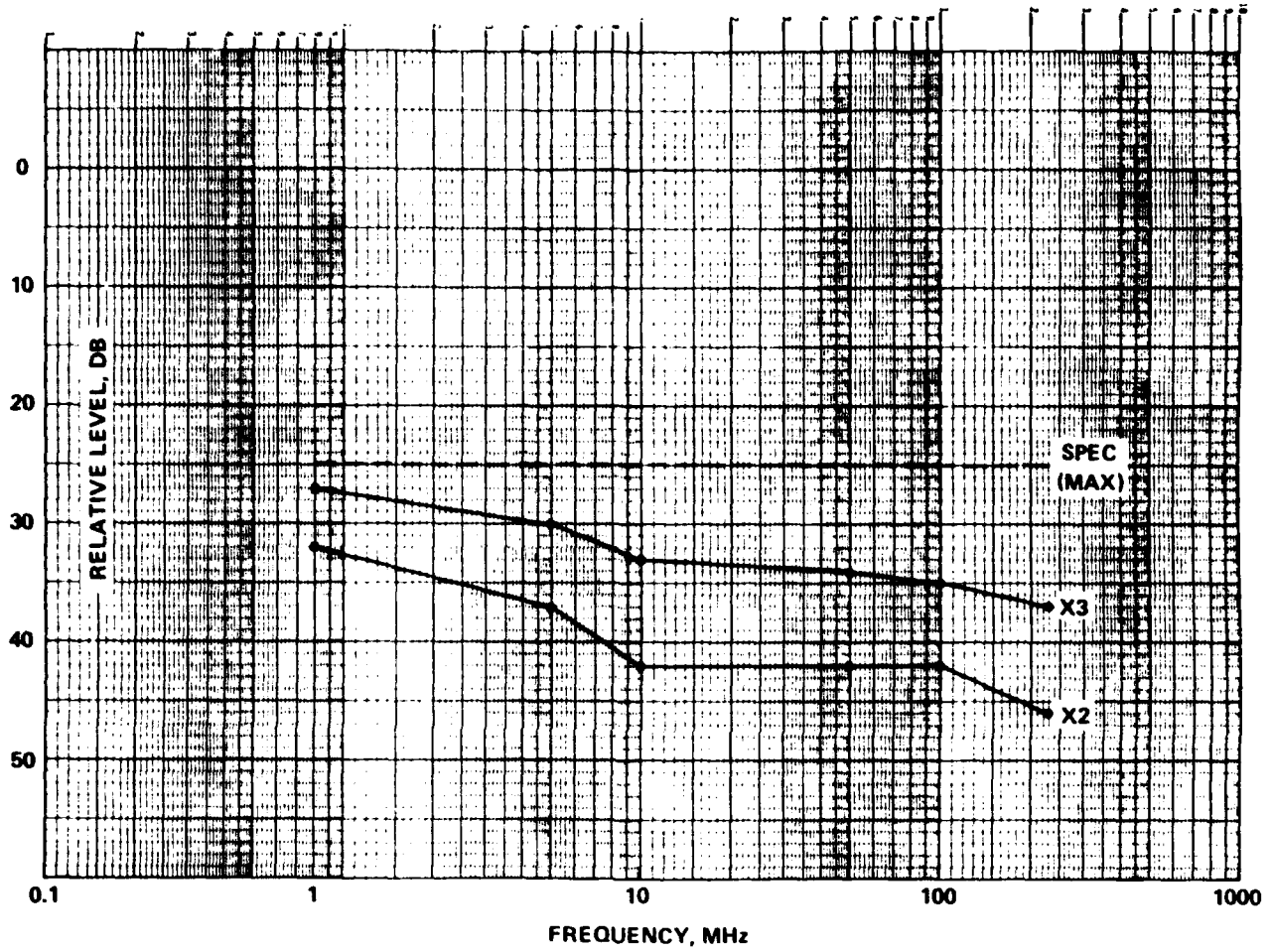


FIGURE 4.3.8.4. RF OUTPUT HARMONIC DISTORTION VS FREQUENCY PLOT

The log mode must have fast response (less than 100 μsec) to signal level changes. Selectivity must be sufficient to ensure that the second harmonic response is more than 40 dB down, that the IF-level-detector ("A" meter) noise is acceptable, and that the unit does not enter log-mode gain compression on noise alone.

The necessity for meeting a variety of demanding requirements resulted in a more complex IF Amplifier circuit than its basic function would ordinarily dictate.

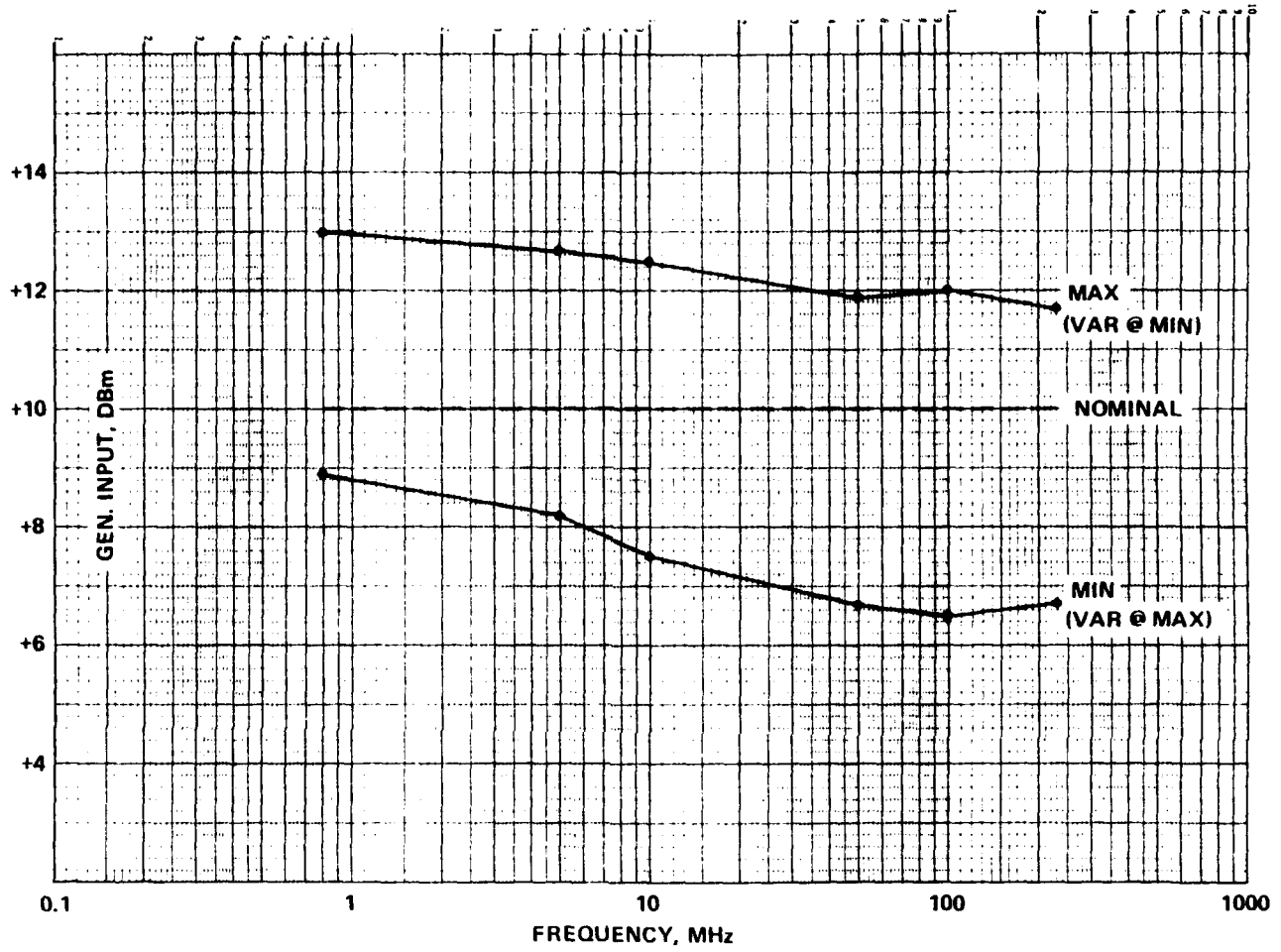


FIGURE 4.3.8.5. GENERATOR INPUT LEVEL LIMITS VS FREQUENCY PLOT

4.4.3 Block Diagram

A Block diagram of the IF Amplifier is shown in Figure 4.4.3. In the MGC mode the signal passes through three-tuned-amplifier stages, each having a gain range of 0 to +40 dB. The third stage is followed by an output buffer which also drives the IF-level ("A") detector and its output amplifier. In the log mode the signal first passes through three non-linear stages which provide a quasi-logarithmic transfer characteristic. The signal then enters the third MGC stage and proceeds through the same output circuits. Three lines are used for external MGC gain and mode programming.

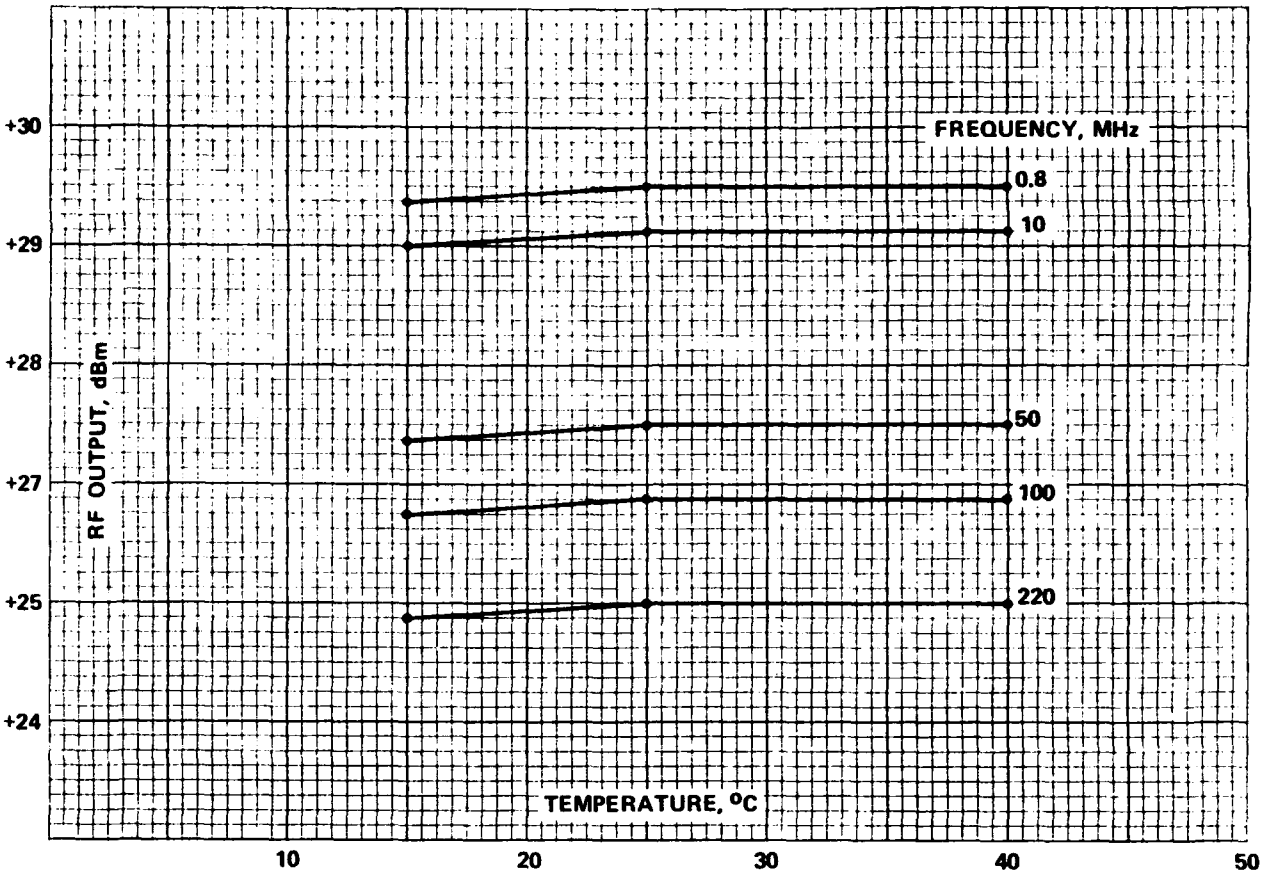


FIGURE 4.3.8.6. RF OUTPUT VS TEMPERATURE PLOT

4.4.3.1 Linear Amplifier Stages

The MGC stages are three essentially identidal J-FET cascode amplifiers as shown in Figure 4.4.3.1. These stages offer nearly ideal characteristics for this application: high gain, low noise, convenient gain control and good signal-handling capability. The stages are quite simple and can be cascaded directly. Each of the three tank circuits has a Q of 20; they are synchronously tuned to give a Gaussian selectivity curve for best transient response. The overall 3-dB bandwidth is 2 kHz. The input noise of the amplifier is about 3 nV/$\sqrt{\text{ Hz}}$ at 80 kHz. With a 1000-ohm source impedance (the value for the receiver mixer) this results in a 2-dB noise figure and an amplifier equivalent input-noise voltage of 0.13 μV rms.

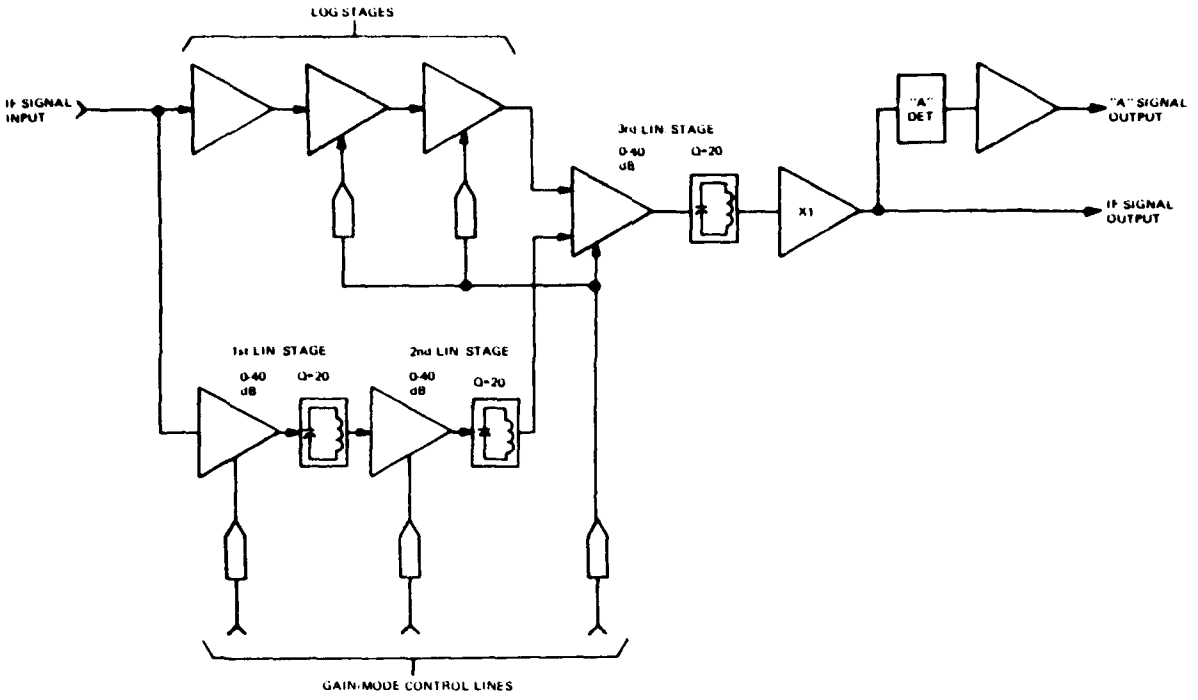


FIGURE 4.4.3. IF AMPLIFIER BLOCK DIAGRAM

The gain of the three MGC stages is programmed in 9 steps of approximately 13 dB; a potentiometer provides continuous control within each step. The gain of the first stage is the last to be reduced, thus insuring the best noise figure. The three programming lines are isolated by voltage followers, RC networks and feed-thru capacitors. The gain-control characteristics are made reproducible by using matched transistors and adjusting the unity gain condition.

4.4.3.2 Logarithmic Amplifier Stages

The log stages are built with IC operational amplifiers and have a basic circuit configuration as shown in Figure 4.4.3.2.1. Small-signal gain is set by resistor R_2. Diode feedback gives the stage unity incremental gain when the output signal exceeds the diode threshold voltage. The parallel-LC tank in the feedback path has two purposes: (1) to avoid a dc offset caused by the amplifier input current, and (2) to provide a slight amount of selectivity

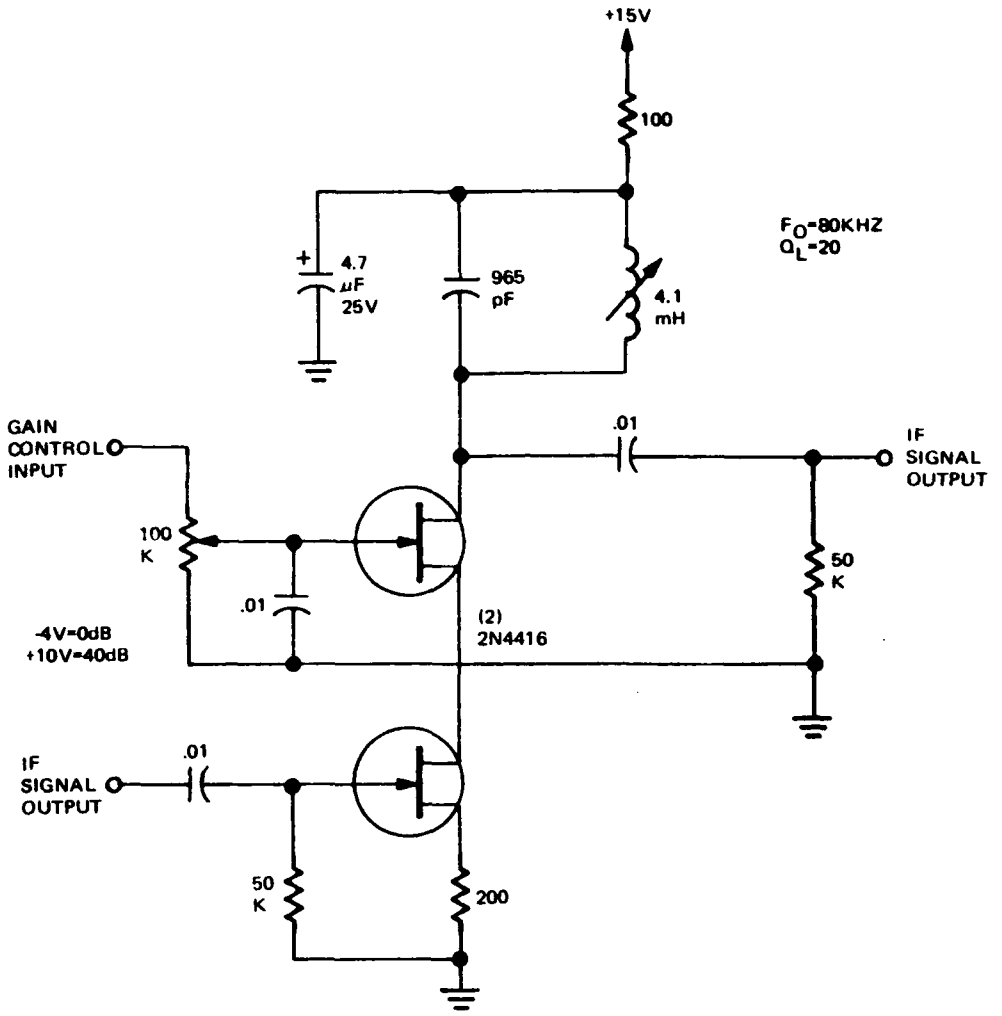
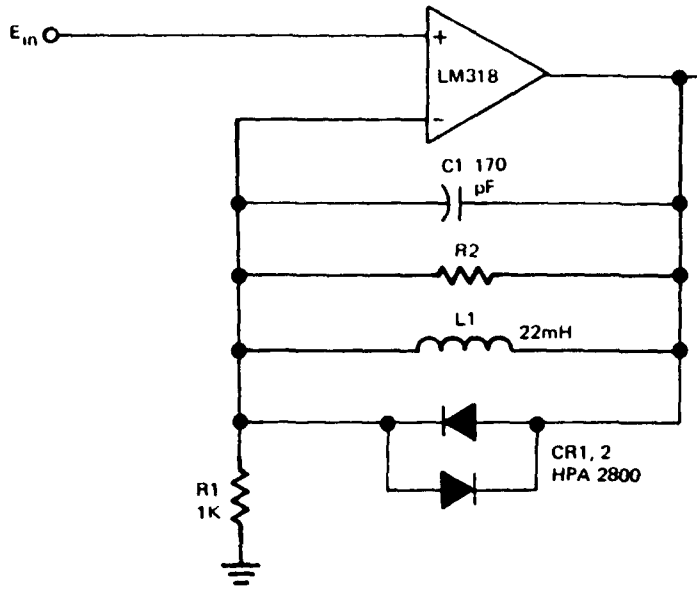


FIGURE 4.4.3.1. J-FET CASCODE AMPLIFIER STAGE

to limit the noise bandwidth. A cascade of these stages provides a highly reproducible quasi-logarithmic characteristic.

The input log stage has a bipolar-transtor differential pair which serves as a low-noise preamplifier. This circuit is shown in Figure 4.4.3.2.2.

The output of the third log stage is applied to the lower gate of another J-FET cascode. This drives the tank circuit used for third MGC stage, thus combining the two signal paths as shown in Figure 4.4.3.2.3.



Total Log Mode Small Signal Gain, dB*	Each Stage R2, K	Each Stage Q
70	15.4	1.3
90	56.2	4.3

*with input log stage as shown in Figure 4.4.3.2.2 and two of these stages

FIGURE 4.4.3.2.1. BASIC LOG STAGE

4.4.3.3 Output Buffer Stage

The output buffer is an IC voltage follower. The "A" output is obtained from a prebiased voltage-doubler negative-peak detector and inverting amplifier as shown in Figure 4.4.3.3. The "A" meter full scale corresponds to an "A" detector output of 1.0 vdc and an IF output of 1.1 V rms.

4.4.3.4 Mode Control

Mode switching is accomplished by sensing the voltage on the third MGC stage gain-control input line. The MGC programming range is from -4V (0 dB) to +10V (40 dB). The three gain-control lines are at -15V for the log mode; this not only disables the MGC stages but also activates the last two log stages and the log cascode, which are "off" for the MGC mode of operation.

4.4.3.5 Transient Response

The transient response of the IF Amplifier is limited only by its selectivity in either mode. The 3-dB bandwidths are 2 kHz in the MGC mode and

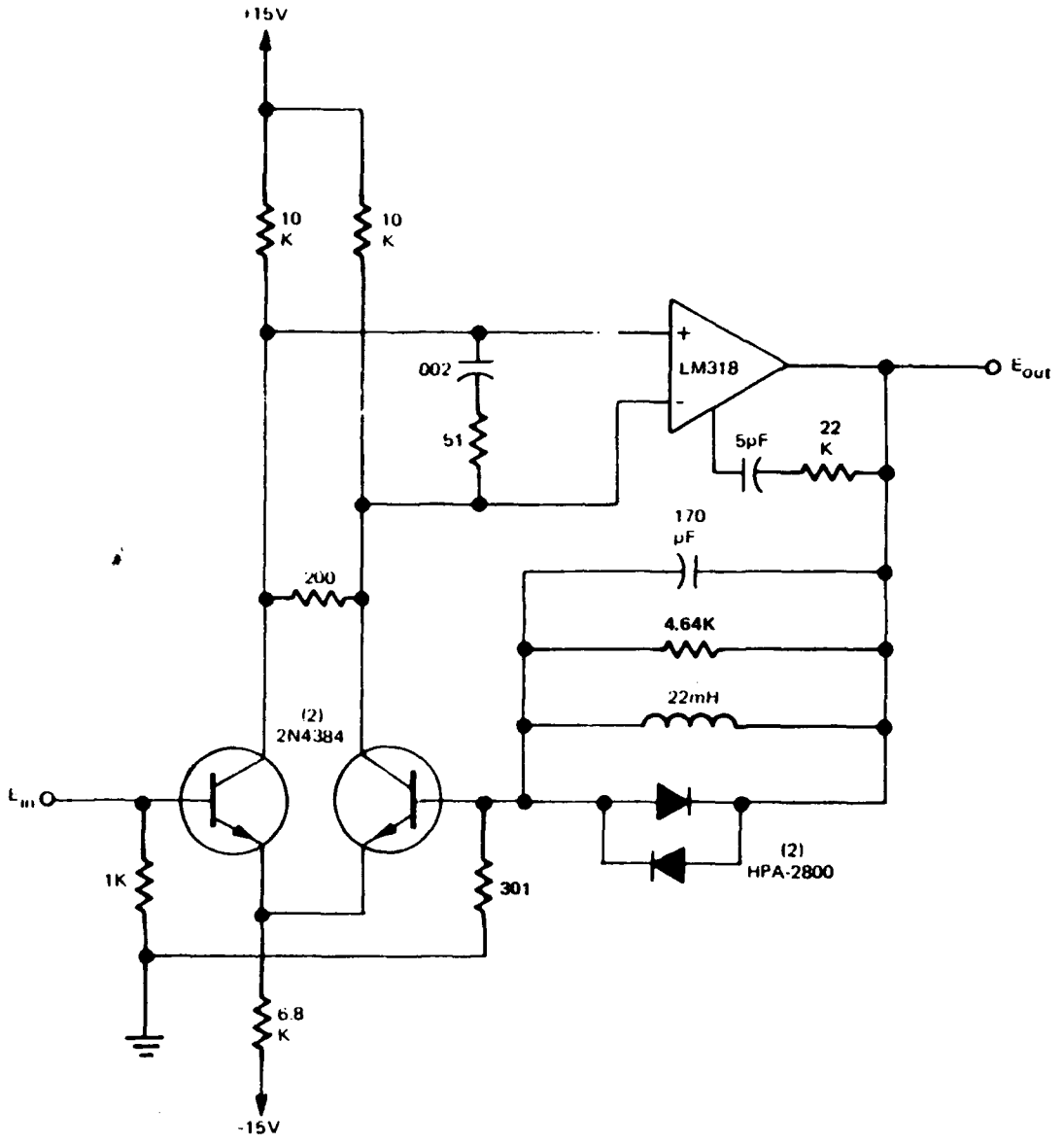


FIGURE 4.4.3.2.2. INPUT LOG STAGE

3.5 kHz in the log mode. These values correspond to time constants of 160 μs and 90 μs, respectively.

4.4.4 Circuit Schematic

The schematic diagram of the entire 80- kHz IF Amplifier is shown in Figure 4.4.4.

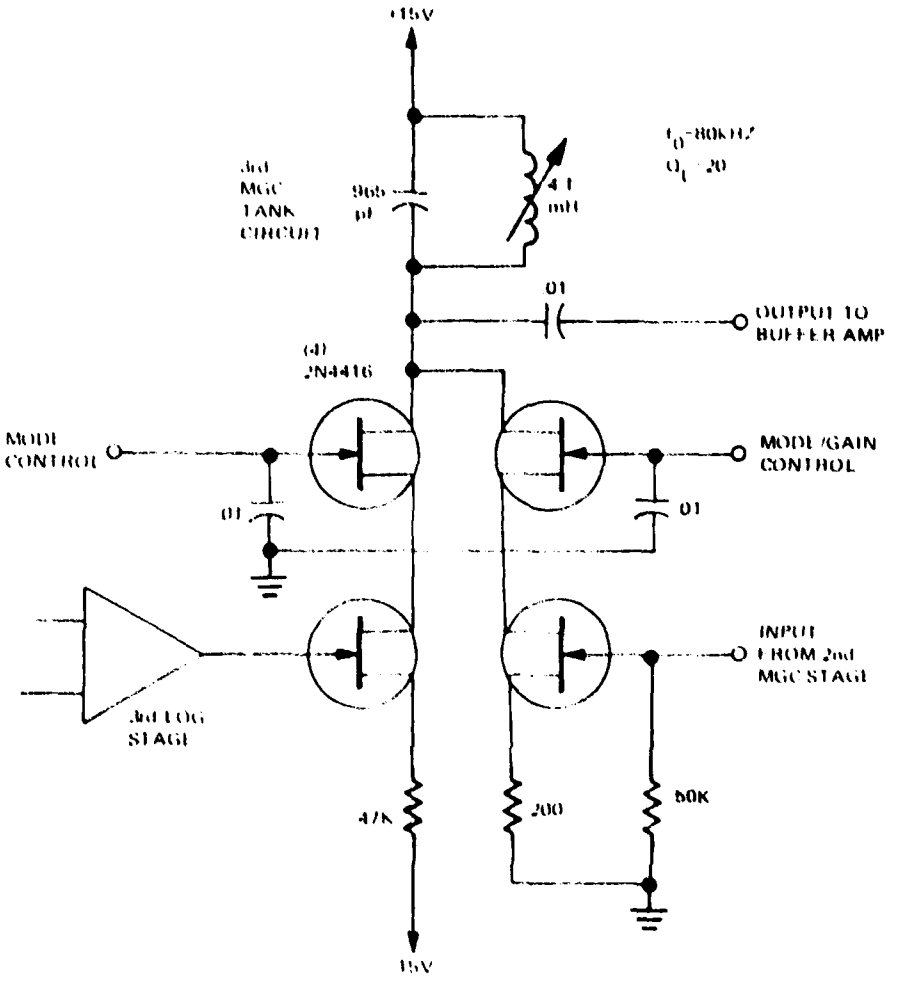


FIGURE 4.4.3.2.3. SIGNAL COMBINING CIRCUIT

4.4.5 Test and Performance Data

The measured performance of the IF Amplifier is shown in Tables 4.4.5.1 thru 4.4.5.4 and Figures 4.4.5.1 and 4.4.5.2. Temperature tests were made over the range of -10^{o}C to $+60^{o}$C. The only significant variations observed were a 4 dB change in the minimum linear mode gain at $+60^{o}$ and a 1% change in the log mode characteristic slope over the complete temperature range.

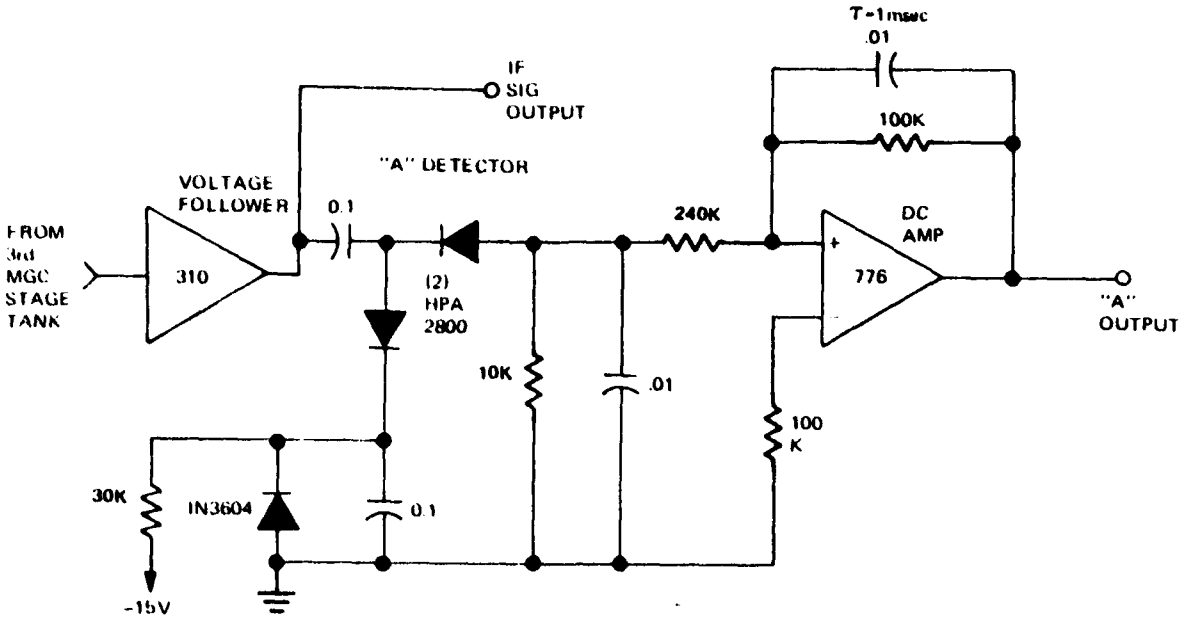


FIGURE 4.4.3.3. OUTPUT CIRCUITS

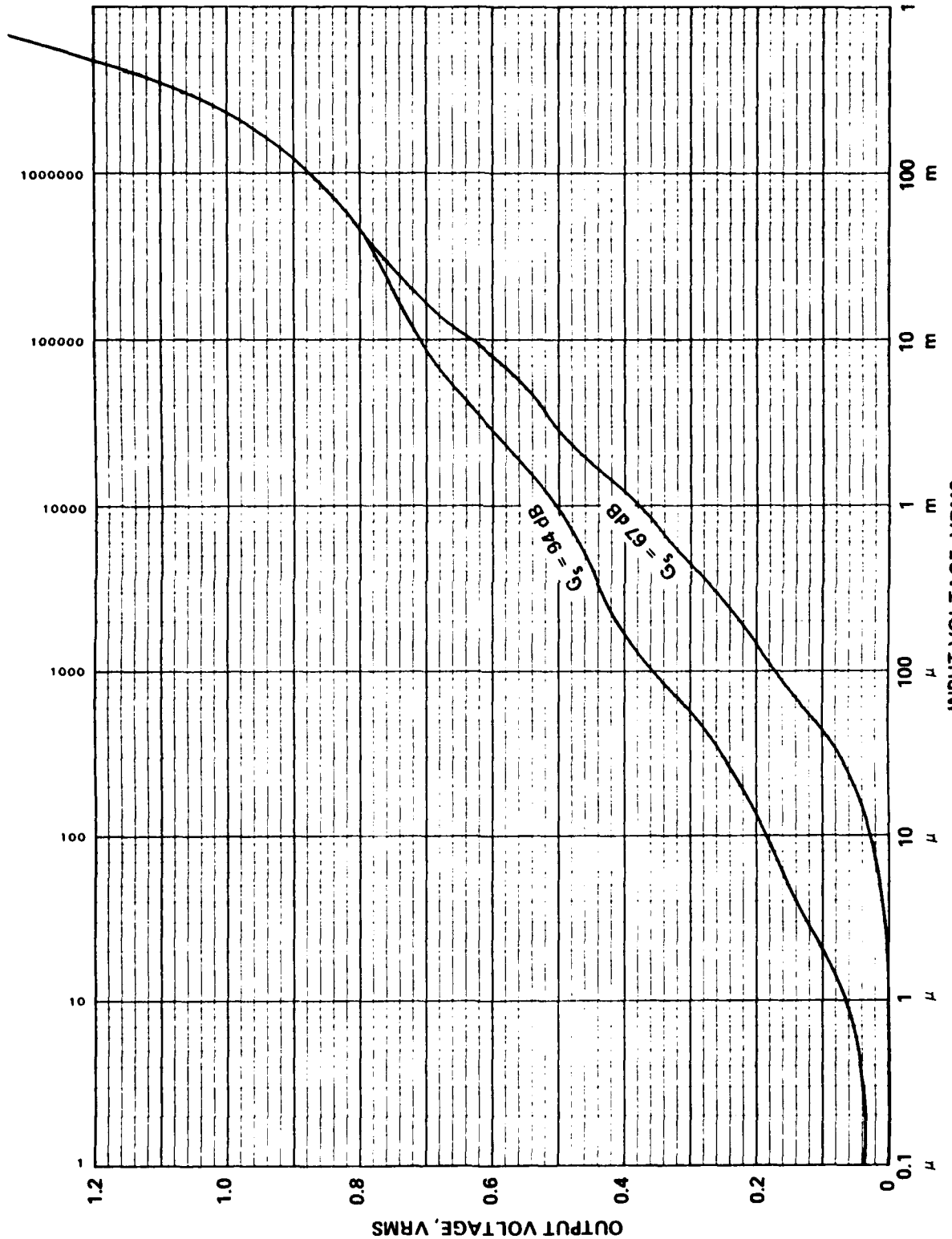
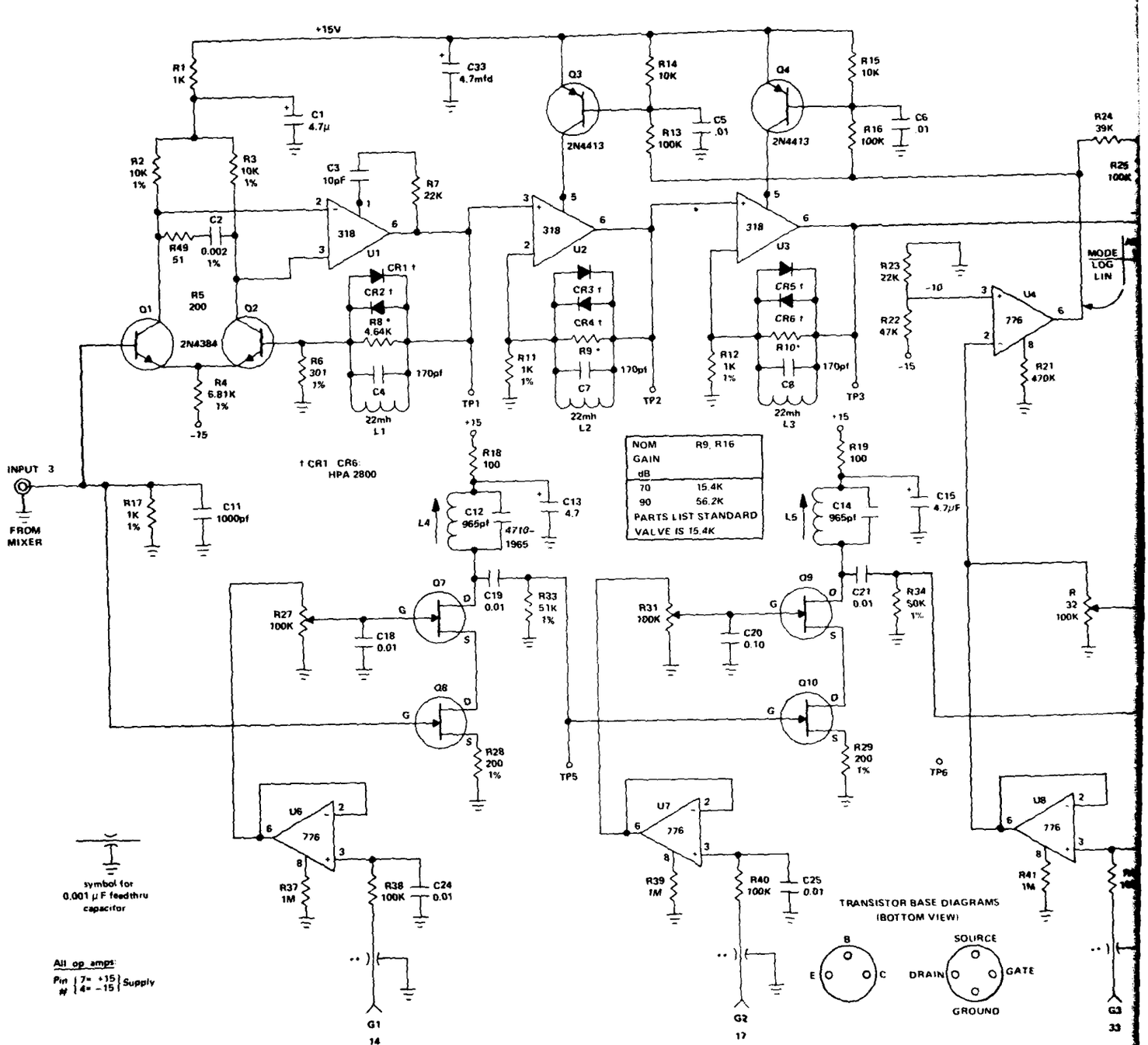


FIGURE 4.4.5.1. LOG IF AMPLIFIER, RESPONSE CHARACTERISTIC



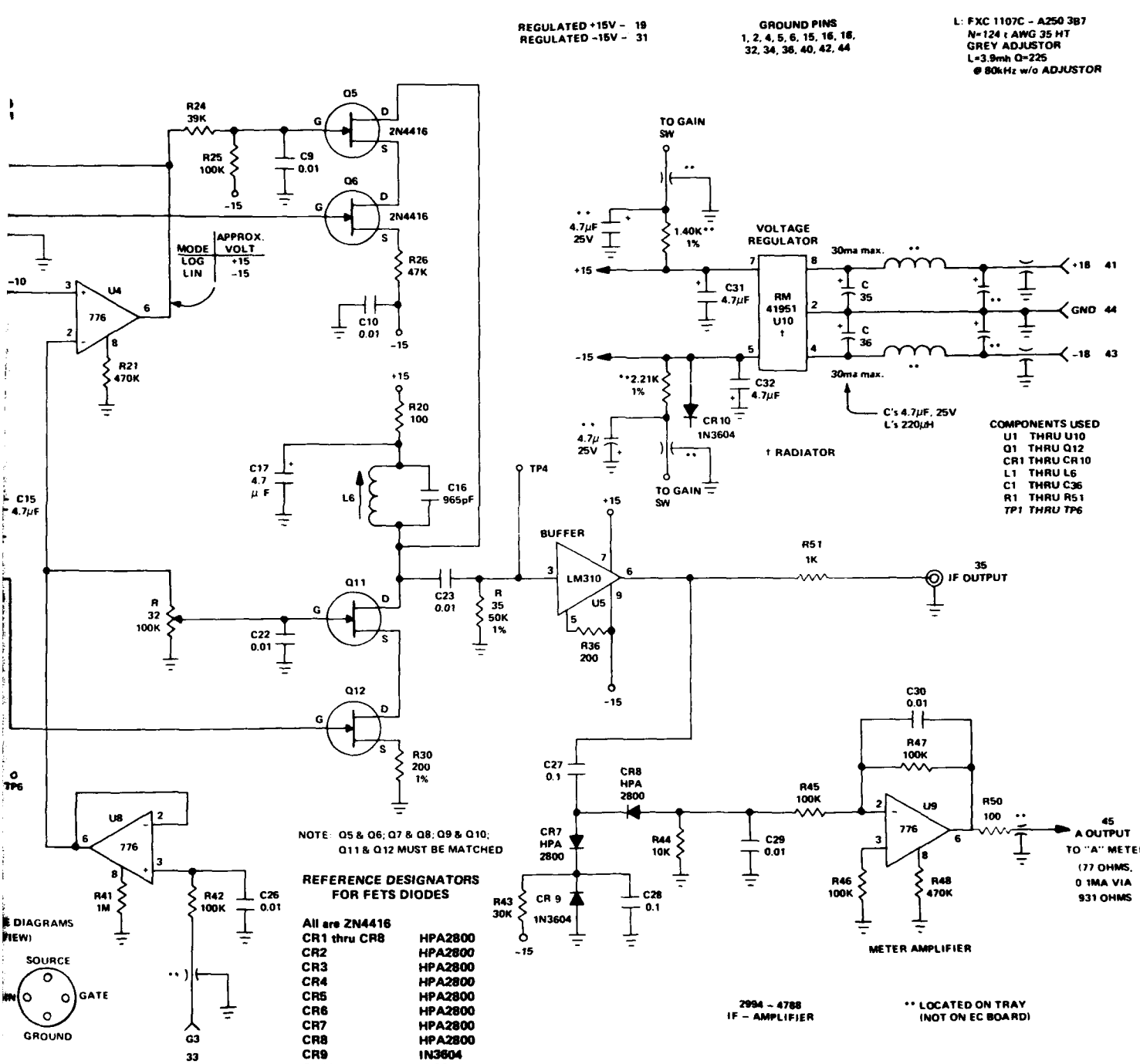


FIGURE 4.4.4. OVERALL IF AMPLIFIER, SCHEMATIC DIAGRAM

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The nominal quasi-log characteristic is shown in Figure 4.4.5.2 for both maximum and minimum small-signal gain adjustments.

Table 4.4.5.1. Lin Mode Performance

Characteristic	Specified	Measured
Gain Range	10-100 dB	0-120 dB ±2 dB
Gain Control	10 position switch with with potentiometer	9 steps of 13 dB nominal with continuous control within each step
Noise Figure *1	3 dB max	2 dB typical *2
Bandwidth (-3 db)	2 kHz	1.9 kHz
Transient Response (Time Constant)	none	160 usec
Relative Gain at 2nd harmonic	≥ 40 dB down	-59 dB
Gain Linearity *3	±5% over 30 dB range	±4% over 50 dB range

Notes:

*1 From 1000-ohm source impedance of signal mixer output port with gain to or greater than 40 dB.

*2 Device selection with 85% yield.

*3 Measured at minimum gain with input signal of 250 mV rms (worst case).

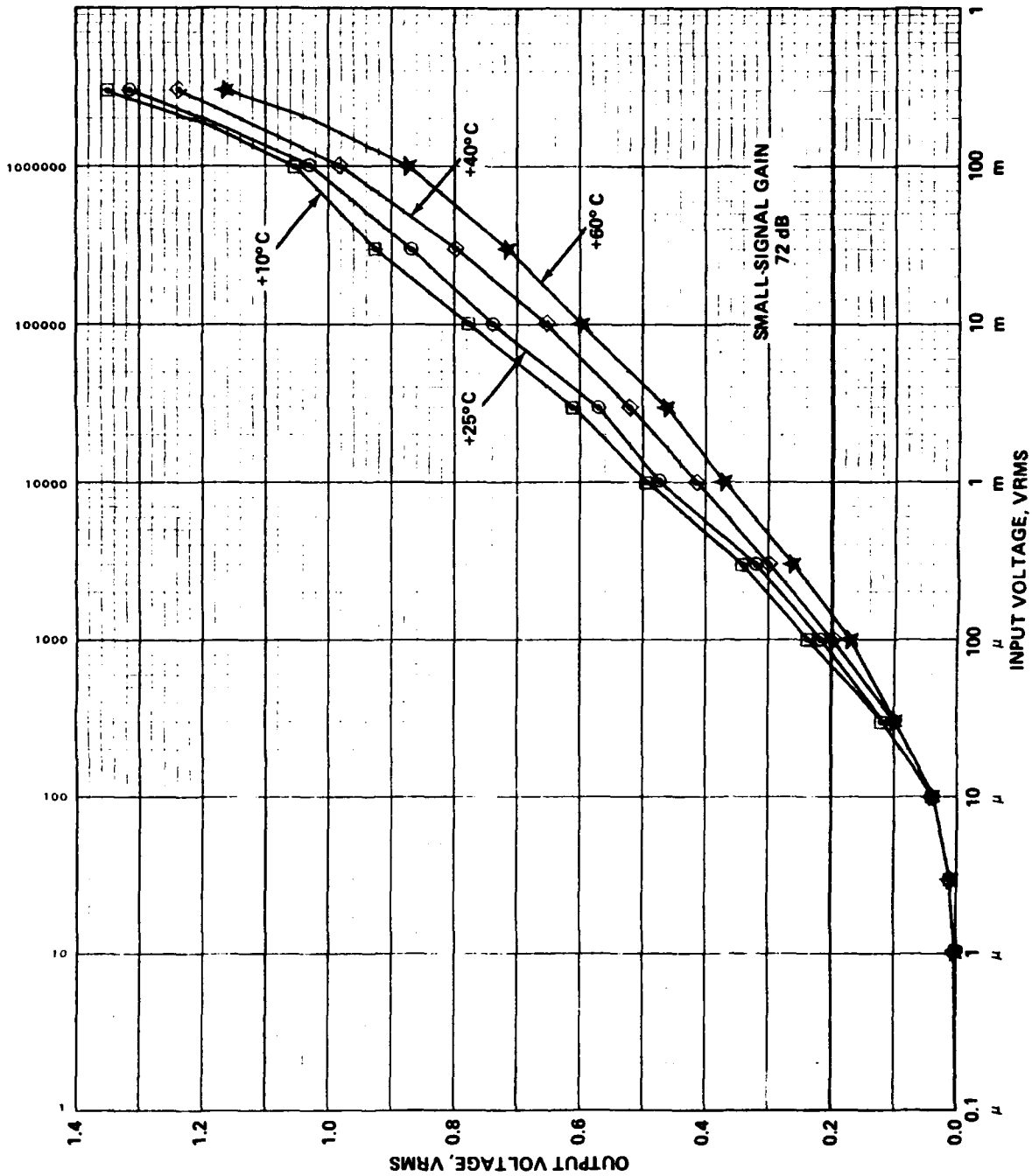


FIGURE 4.4.5.2. LOG MODE CHARACTERISTIC VS. TEMPERATURE PLOT

Table 4.4.5.2. Log Mode Performance

Characteristic	Specified	Measured
Small-signal Gain Adjustment Range	70-100	70-100 dB ±2 dB
Response	quasi-logarithmic over 60 dB range	quasi-logarithmic over entire dynamic range 70-100 dB
Noise Figure *1	3 dB max	2.5 dB typical
Bandwidth (-3 dB)	none (3.5 kHz design)	3.4 kHz
Transient Response (time constant)	100 μsec	90 μsec
Output Harmonic *2 Distortion	none	X2 - 53 dB X3 - 48 dB Higher - 60 dB

Notes:

*1 From 100-ohm source impedance of signal mixer output port and all gain and signal conditions.

*2 Maximum relative level for any input level up to 1V rms.

Table 4.4.5.3. General Performance

Characteristic	Specified	Measured
Input signal Maximum *1	-	0.5 rms
Output Signal Maximum *2	2.5V pp	5V pp
"A" Meter Scale	1.5V pp FS	1.1V rms FS *3
"A" Meter Time Constant	0.1 sec.	approx 0.1 sec. *4
"A" Output Time Constant	1 msec	1.2 msec
"A" Output Scale Factor	-	1.0 VDC FS

Notes:

*1 Input signal positive peak clipping occurs above this level in either mode.

*2 Output signal negative peak clipping occurs above this level in either mode. Maximum clipped output swing under overload conditions is 27V pp. The synchronous detector module contains zener diodes to limit this to approx. 6V pp.

*3 This value is required for compatability with synchronous detectors.

*4 Determined by meter itself.

Table 4.4.5.4. Power Consumption

Mode	Supply Current mA	
	+18V supply	-18V supply
Log	32	32
Lin	28	27

Total Power 1.2W

4.4.5.1 Other Characteristics

1. Nominal Phase shift through IF Amplifier is 180^{o} in both lin and log modes.
2. Typical variation in IF Amplifier phase shift in linear mode is $\pm 5^{o}$ for entire gain range.
3. Typical variation in IF Amplifier phase shift in linear mode is $\pm 4^{o}$ for all input levels within dynamic range.
4. Typical variation in IF Amplifier phase shift in linear mode is $\pm 5^{o}$ for + 10^{o}C to + 60^{o}C temperature range.

4.5 Sweep and Servo Amplifier Module

4.5.1 General

This module provides the operating controls and signals for displaying crystal responses as a function of applied frequency as well as signal conditioning for locking the frequency source to a null in the "X" output of the quadrature synchronous detector. A mode switch selects (1) a sawtooth sweep voltage applied to frequency source, (2) a center frequency adjustment for manual operation, (3) a locked mode where the "X" output is integrated and applied to frequency control to null its output and (4) and automatic acquisition mode. A simplified diagram is shown in Figure 4.5.1.

In the sweep mode, a variable rate and variable amplitude sawtooth voltage is applied to the synthesizer frequency control. A constant $\pm$10V sawtooth provides the horizontal sweep voltage for oscilloscope display. The vertical output is the "A" detector or the total bridge unbalance signal.

The center mode provides manual setting of the synthesizer frequency with the center control potentiometer. Manual sweeps are possible

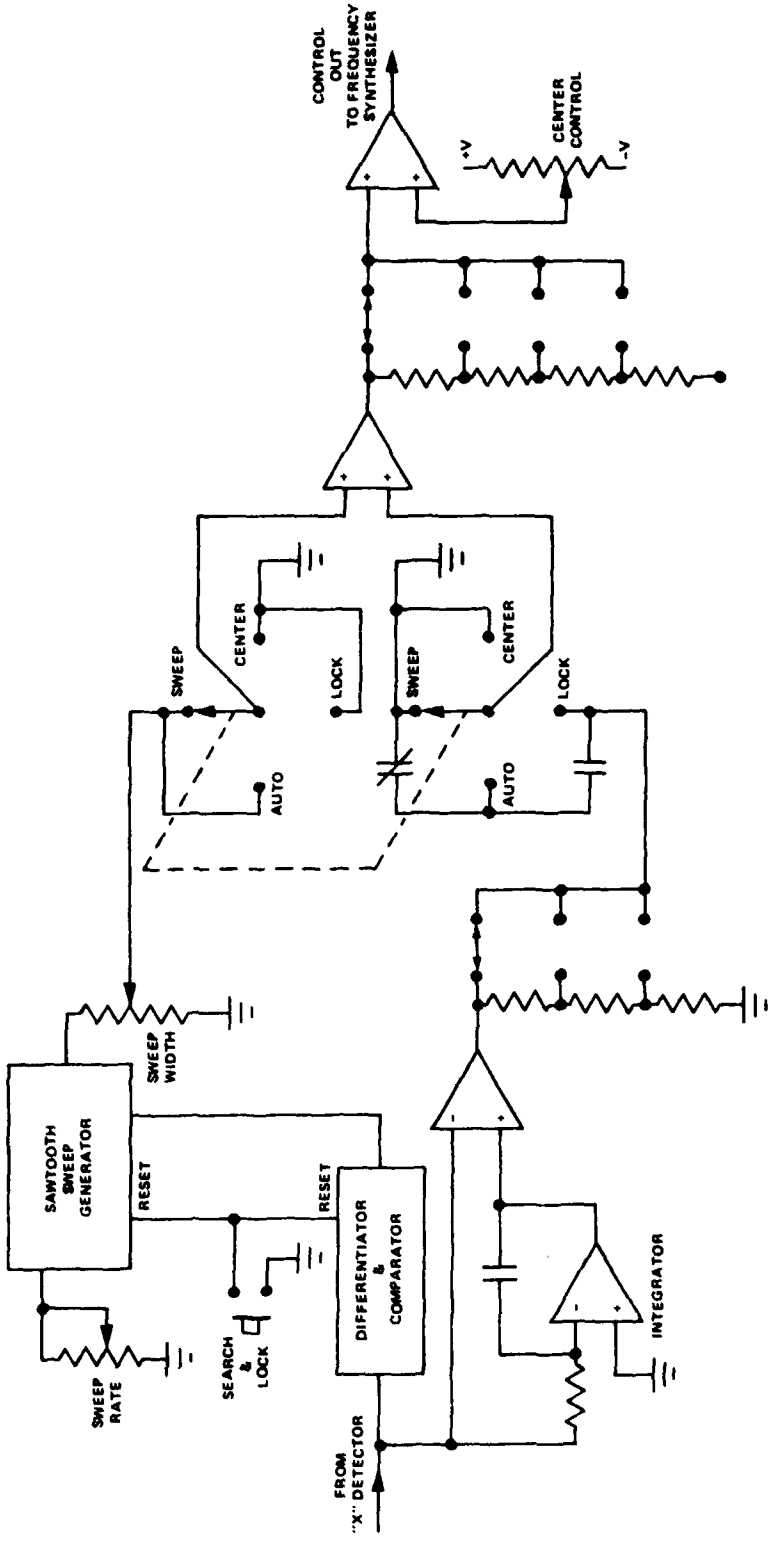


FIGURE 4.5.1. SWEEP AND SERVO AMPLIFIER MODULE, SIMPLIFIED SCHEMATIC DIAGRAM

with this control. The center control provides centering adjustment in all modes allowing manual nulling as well as sweep centering.

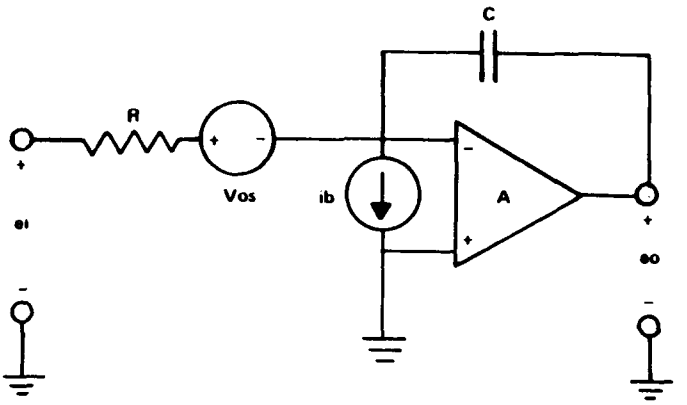
Locking the servo bridge is done in the lock mode by applying the sum of the "X" detector output and its integral to the frequency control. When proper phasing and gain adjustments are set the servo amplifier will null the "X" output. The servo will keep the "X" output nulled for small changes in frequency and bridge unbalance.

The automatic acquisition mode starts a sweep beginning at the lowest frequency when the search and lock button is released. The sweep continues until a response detected by a differentiator on the "X" output stops the sweep, and switches to the lock mode. The sweep voltage is held constant at the value that tripped the differentiator and comparator. The integrator provides the dc gain necessary to reduce the "X" detector output to zero. Attentuators at the control output and "X" detector integrator output allow the servo gain to be set to maximize the bridge sensitivities and ease balancing.

4.5.2 Design Considerations

Two areas of particular difficulty in the design of the sweep and servo amplifier were the integrating amplifier and the sawtooth sweep generator.

The output voltage of an active integrator is shown in Figure 4.5.2. The only desired term is the first term. The error terms consist of both fixed value terms and terms which increase with time. The fixed voltage errors can be made very small by using a high performance operational amplifier. The remaining error terms which are integrated with time along with the desired output are difficult to reduce.



$$e_o = -\frac{1}{RC}\int_o^t e_i dt \quad \frac{1}{RC}\int_o^t \frac{e_o}{A}\,dt + \frac{1}{RC}\int_o^t Vos\,dt + \frac{1}{C}\int_o^t ib\,dt - \frac{e_o}{A} + Vos$$

where

A = gain of operational amplifier

Vos = offset voltage of op amp

i_b = bias current of op amp

FIGURE 4.5.2.1. ACTIVE INTEGRATOR, PARAMETRIC DIAGRAM

When the tracking servo bridge detector is operated in the lock mode, the control output voltage error is caused by these integrator error terms plus any fixed offset voltage introduced by following amplifiers. The requirement that the control output voltage not change by more than one millivolt in 30 seconds with the input grounded is not practical to meet with any degree of reliability over more than a few degrees of temperature range.

Ignoring the signs of error terms (since the directions chosen for V_{os} and i_b are arbitrary) each parameter of the operational amplifier (A, V_{os}, and i_b) must not exceed the value given in Table 4.5.1 in order for this term not to contribute more than the total error budget all by itself. The resistor is 2 megohms and the capacitor 1.0 uF giving the 2 second time constant. The maximum value of E_o is 1.0 volt, corresponding to maximum permitted control output voltage.

Table 4.5.1. Active Integrator Parameters

Term	Parameter	Required Value	Comment
$\frac{1}{RC}\int \frac{e_o}{A}\,dt$	A	1500	no problem
$\frac{1}{RC}\int V_{os}\,dt$	V_{os}	67 uV	difficult - requires careful trimming
$\frac{1}{C}\int i_b\,dt$	i_b	33pA	requires good FET op amp
$\frac{e_o}{A}$	A	1000	no problem
V_{os}	V_{os}	1 mV	no problem

To satisfy these requirements a hybrid precision FET operational amplifier such as the Burr-Brown 3521L must be used. The key parameter specifications for the 3521L are:

A	50,000 min
V_{os}	$\pm$250 uV max untrimmed
TC of V_{os}	$\pm$1 uV/^{o}C max
i_b	$\pm$10 pA max at 25^{o}C

The above specifications show that the offset voltage term is the parameter of concern. A ten to one improvement is obtained with an external trimming network. A trimmed offset voltage of 25 uV will equal the contribution of the temperature coefficient of the offset voltage over the entire +15^{o}C to +40^{o}C ambient range.

The total worst case error voltage at the output of the integrator using the 3521L, trimmed to 25 uV offset voltage, after 30 seconds is 0.5 mV.

Trimming of V_{os} to 50 uV is required to meet the specification.

The sawtooth sweep generator is subject to the same limitations as the integrator. To achieve the sweep rate of 50 sweeps per second the sawtooth generator integrator must be 200 times faster. Thus the time dependent error terms accumulate at 200 times the rate for the integrator. For sweep displays of the crystal response these errors are negligible.

For operation in the auto lock mode the sweep output is stopped and held at the value giving the lowest frequency crystal response. This voltage is summed with the integrator output to produce the synthesizer control voltage. Since it is this control output voltage we wish to hold constant once the servo bridge has locked on the crystal resonance, we can see that the sawtooth sweep generator errors are as important as the integrator errors in lock mode.

With the time dependent error terms increasing at 200 times the rate for the integrator, even more stringent requirements are placed on the op amp used in the sweep generator. Since this is not practical with devices available, the analog sweep generator was abandoned. In its place a digitally derived sweep generator was designed. A simplified diagram of the digital sweep generator is shown in Figure 4.5.2.2.

The design principle is to derive the sweep voltage from the output of an 8-bit counter with a digital-to-analog converter. The sweep therefore consists of 256 steps. The CMOS counter directly drives the R-2R thin film microelectronic resistor network since the output swings are within a few millivolts of the supply voltages for the counter. The counter is reset to zero when the search and lock button is depressed. This starts the sweep

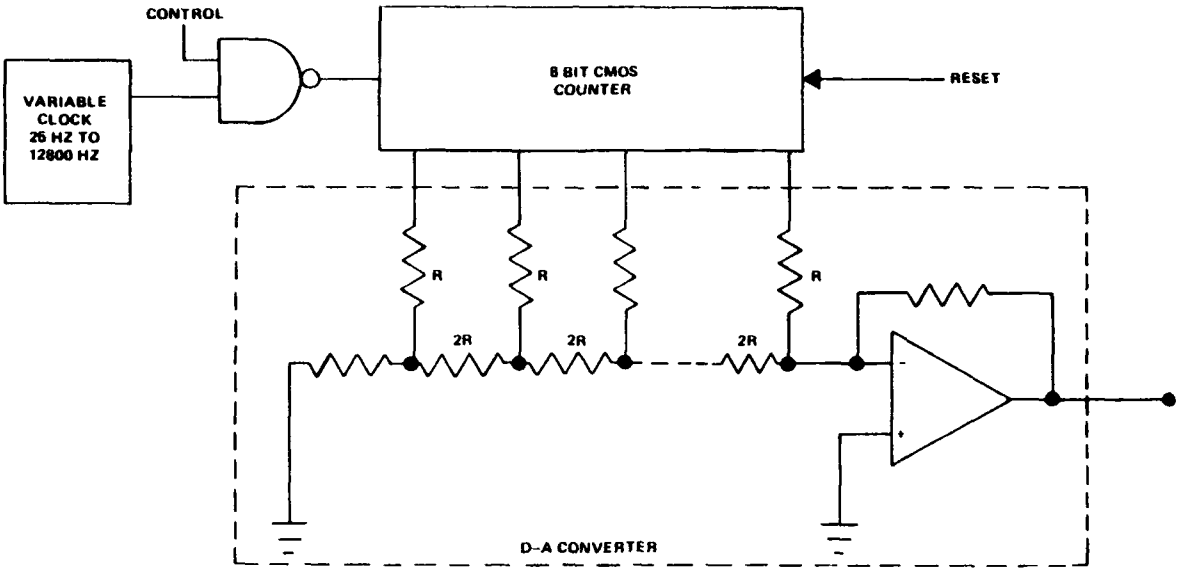


FIGURE 4.5.2.2. DIGITALLY DERIVED SWEEP GENERATOR, SIMPLIFIED SCHEMATIC DIAGRAM

at the voltage corresponding to the low frequency end of the synthesizer sweep range. The counter counts the clock pulses until a signal is detected by a differentiator on the "X" synchronous detector output. At this point the clock output is cut off by the NAND gate and the counter holds the value corresponding to the first cyrstal response detected. This valve is held until another search and lock sequence is initiated or another mode is selected. No time dependent error terms are present since no actual integration takes place.

The variable clock consists of a precision timer, LM 322, and a unijunction transistor for resetting the timer. A logarithmic potentiometer is used to allow ease of setting the sweep rate over 500 to 1 range.

4.5.3 Sweep Generator

The sweep generator provides a linear ramp voltage to sweep the synthesizer frequency. In the AUTOMATIC mode, the sweep signal must stop when

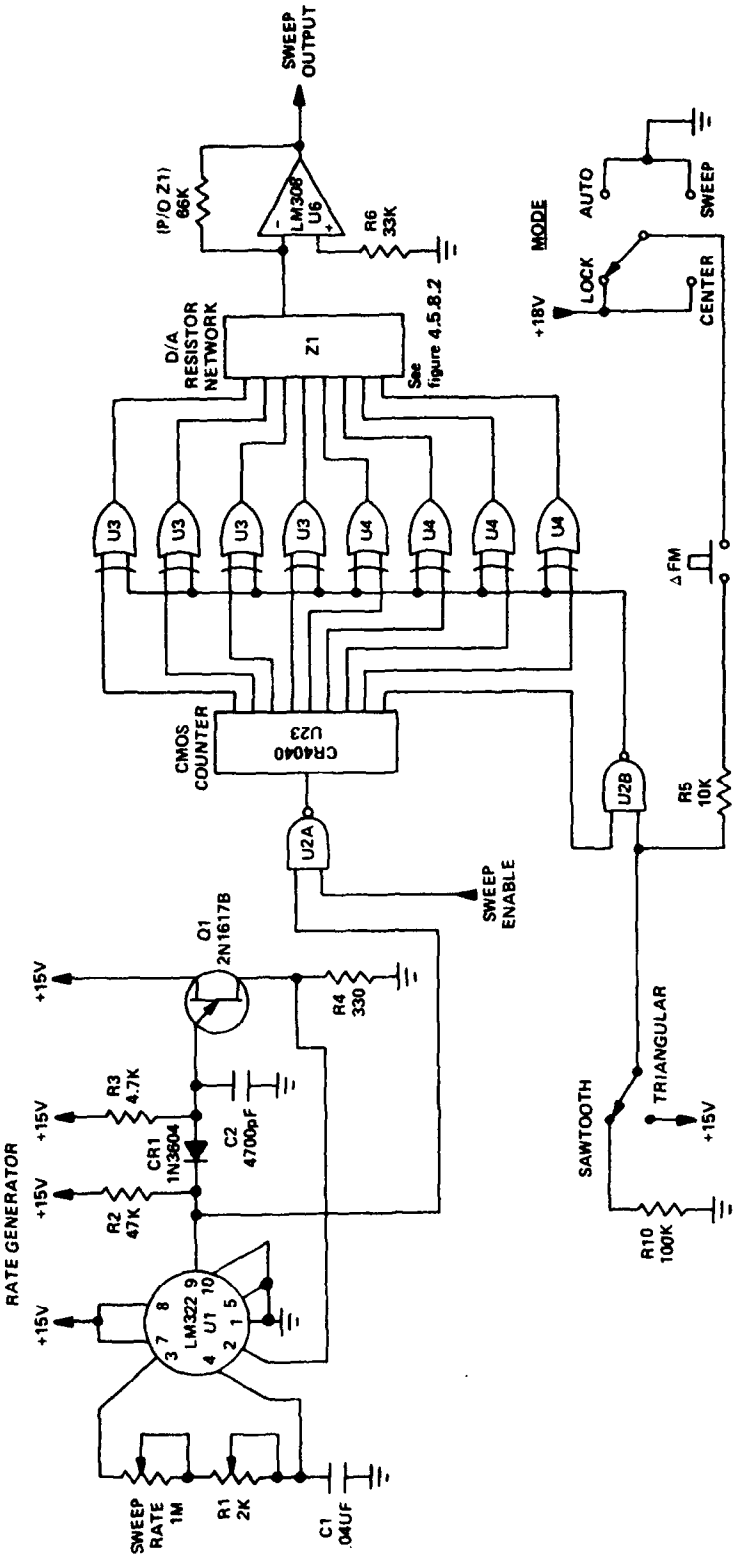


FIGURE 4.5.3. SWEEP GENERATOR, SIMPLIFIED SCHEMATIC DIAGRAM

the measurement is made. To eliminate drift in the "stopped" sweep voltage, a digitally derived sweep voltage is used. The linear ramp voltage consists of 256 small steps. These steps are derived from the output of a CMOS counter driving a D-A converter. A diagram of the sweep voltage generator is shown in Figure 4.5.3.

The precision timer U1 and unijunction transistor (Q1) network make up an adjustable rate generator from 25.6 Hz to 12.8 kHz. The 1 Megohm SWEEP RATE control has a counterclockwise logarithmic taper to allow convenient setting of the sweep rate over the 500 to 1 adjustment range. Trimmer resistor R1 is adjusted in the final instrument to give the correct maximum sweep rate when the front panel control is set for minimum resistance. This takes up the variation in the minimum resistance of the 1 megohm control.

The LM322 precision timer output, pin 9, goes positive at the completion of the timing cycle. This allows C2 to begin charging through R3 until the threshold of the unijunction transistor is reached. At this point C2 is dischared by the UJT through R4, applying a reset pulse to the trigger input of the timer (pin 2). Diode CR1 isolates the UJT from the positive swing of the timer output. Resistor R2 provides pull-up for the collector of the timer output transistor.

These output pulses drive the clock input of twelve bit CMOS counter U23 through gate U2A. This NAND gate provides control by permitting the clock pulses to be stopped when a crystal response is detected in the AUTOMATIC mode. By stopping the counter, the sweep is stopped and the D/A converter holds this sweep voltage. Eight bits of the counter output are applied to the D/A converter resistor network through eight EXCLUSIVE OR gates,

U3 and U4. The resistor network along with the 66K gain determining resistor are a thin-film resistor network on one substrate. The D/A converter resistor network Z1 is an R/2R ladder network containing the resistors that go to the gate outputs with values corrected to include impedance of the gate. The D/A converter resistor network Z1 is an R/ZR ladder network of resistors connected to the exclusive OR gate outputs. The network is shown in Fig. 4.5.8.2. Here R equals 50KΩ and 2R equals 100KΩ . However, since the exclusive OR gates have approximately 500Ω output impedance, the actual 2R resistor values on the network are made 99.5KΩ so that the combined resistance of the gate and the network equals 100KΩ. A 66KΩ resistor in Z1 provide the feedback for the amplifier A 100K resistor. Op-amp U6 sums the D/A output current and transforms it into the sweep voltage.

The function of the EXCLUSIVE OR gates is to allow selection between triangular and sawtooth waveforms. When the waveform selector switch in in the sawtooth position, NAND gate U2B is disabled and the output is high. The counter outputs are then inverted by the EXCLUSIVE OR gates and drive the D/A converter. When the waveforms selector switch is in the triangular position the NAND gate is enabled. The other input to this gate is the counter output at one-half the rate of the most significant bit. Thus at one-half the fundamental rate, one input of the EXCLUSIVE OR gates is alternately high then low. This causes counter output to be alternately inverted then non-inverted, producing a triangular waveform at one-half the rate of the sawtooth waveform. Thus, two waveforms are available for sweeping the synthesizer, with the triangular waveform having one-half the repetition rate of the sawtooth waveform.

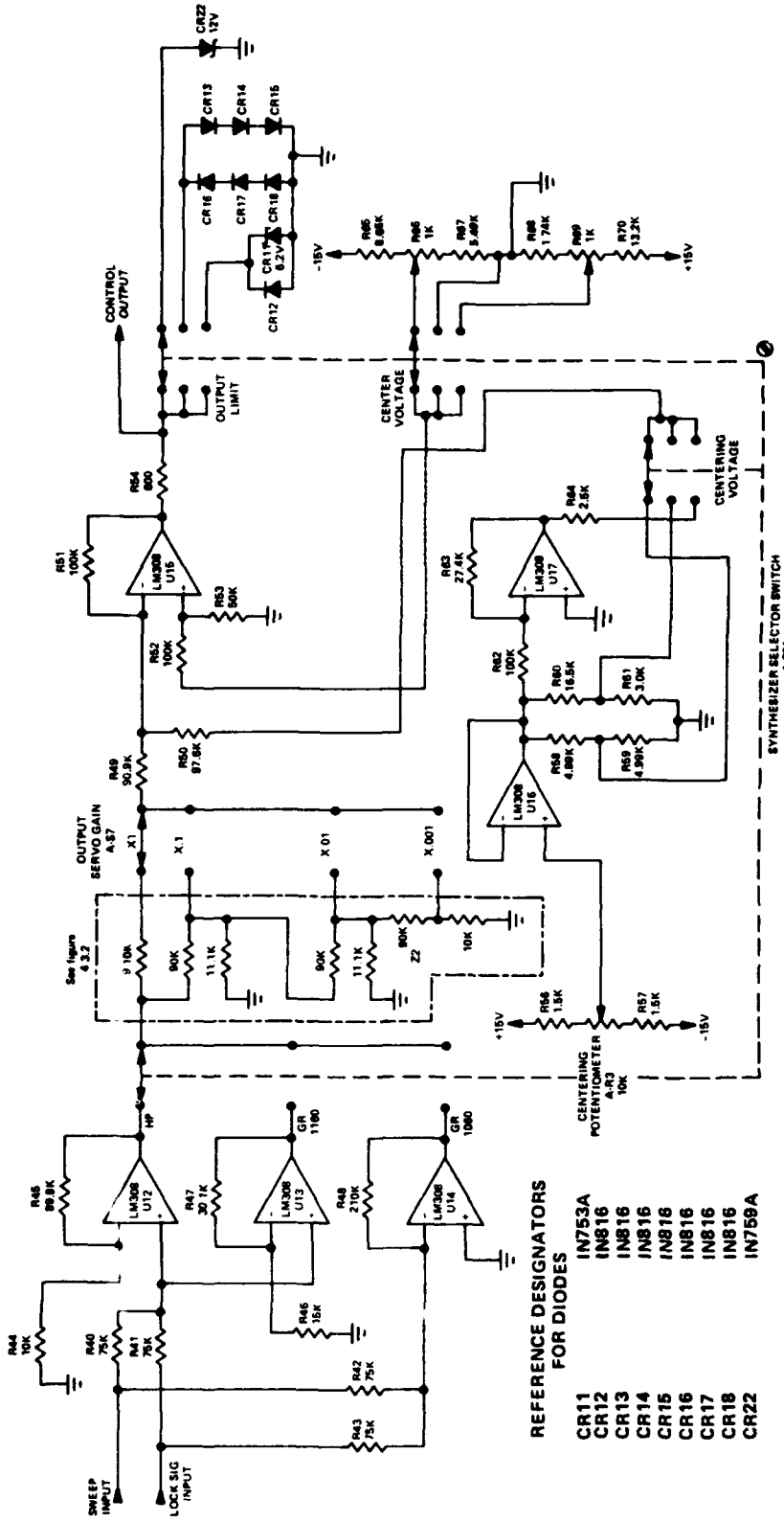
When the Δ FM pushbutton is depressed, the triangular waveform is automatically selected as long as the pushbutton is held.

The sweep output of U6 is used for synthesizer sweep and for providing horizontal sweep voltage for the display oscilloscope. The amplitude of the synthesizer sweep voltage is adjustable by front panel WIDTH control R-2B up to a maximum of slightly greater than one decade of frequency for each of the three synthesizer types. The amplitude of the oscilloscope horizontal sweep is adjustable by rear panel control A-R22 labeled SWEEP AMPLITUDE up to a maximum of $\pm$10V. This allows the sweep display to be adjusted to exactly fill the screen of the oscilloscope.

4.5.4. Synthesizer Control Amplifiers

To accomodate the three common synthesizer types with their different control voltage sensitivities and polarities, three separate op amps are used to sum the sweep voltage and lock signal inputs. These amplifiers along with final output circuits are shown in Figure 4.5.4.

The synthesizer signal amplifiers U12, U13, and U14 convert the sweep voltage and lock signal into the proper polarity and magnitude. Op amp U12 supplies a maximum sweep signal of 10 V peak-to-peak in a non-inverting configuration for the Hewlett Packard series of synthesizers. Op amp U13 supplies a maximum sweep signal of 3 V peak-to-peak in a non-inverting configuration for the General Radio 1160 series synthesizers. Op amp U14 supplies a maximum sweep signal of 5.0 V peak-to-peak in the inverting configuration for the General Radio 1060 series synthesizers. By using a separate amplifier for each synthesizer, switching of low level signals at the op amp input is avoided. The synthesizer selector switching is now done at the output of the op amp where the impedance is low and the signal level is higher than at the input. Thus the circuit is less susceptible to noise pick-up.



REFERENCE DESIGNATORS FOR DIODES

CR11	IN753A
CR12	IN816
CR13	IN816
CR14	IN816
CR15	IN816
CR16	IN816
CR17	IN816
CR18	IN816
CR22	IN759A

FIGURE 4.5.4. SYNTHESIZER CONTROL AMPLIFIERS, SIMPLIFIED SCHEMATIC DIAGRAM

In addition to selecting the proper amplifier, the synthesizer selector switch A-S21 selects the centering control range, the dc center voltage and the output voltage limiter. The centering potentiometer A-R3, a ten turn 10K front panel control, is used for manual sweep as well as control of the center voltage at the control output. The output of centering potentiometer A-R3 drives op amp U16 connected as a voltage follower. Resistive dividers at the output provide the proper adjustment range of the Hewlett Packard and GR 1160 series synthesizeres. The GR 1060 series synthesizers require a polarity reversal, so another op amp U17 is used as an inverter with the proper gain. The centering potentiometer control range is 1.15 times the nominal full decade control range for each synthesizer.

In addition to the adjustable centering control a fixed center voltage provides the center point about which all control output voltages occur. These voltages correspond to the center of the synthesizer control range. These voltages are derived from the $\pm$15 volt power supplies by adjustable voltage dividers, consisting of resistors and potentiometers R65 through R70. The center voltage for each synthesizer series is:

HP	-6.0V
GR 1160	0.0 V
GR 1060	+2.25 V

To limit the voltage swing of the control output to safe values for each synthesizer, limiting diodes CR11 through CR18 and CR22 are placed across the output of U15. The nominal limits for each synthesizer are:

HP	+0.6 V to -14.0 V
GR 1160	-2.4 V to +2.4 V
GR 1060	-0.6 V to +6.2 V

An output attenuator with four decade steps (OUTPUT SERVO GAIN switch A-S7) provides reduction in overall servo gain without affecting the center voltage. The output attenuator network Z2 provides a constant output

impedance when driven from a voltage source. This assures no dc voltage change at the output when the attenuator position is changed. The network is a thin-film resistor network.

The final output amplifier U15 is an op amp with differential input connection. The output voltage is the center voltage minus the sum of the sweep signal + locking input signal + centering adjustment voltages. This provides proper phasing for correct operation.

4.5.5 Integrator and Lock Amplifier

The integrator and lock amplifier provides the feedback to allow the detector to lock a synthesizer on a crystal response and track any frequency disturbances. Figure 4.5.5 gives details of these circuits. The lock signal generated for the synthesizer control with the integrator enabled is:

$$e_{lock} = - e_x \left[\frac{1}{(1 + j\omega R33\ C9)} + \frac{1}{j\omega\ R24\ C8} \right]$$

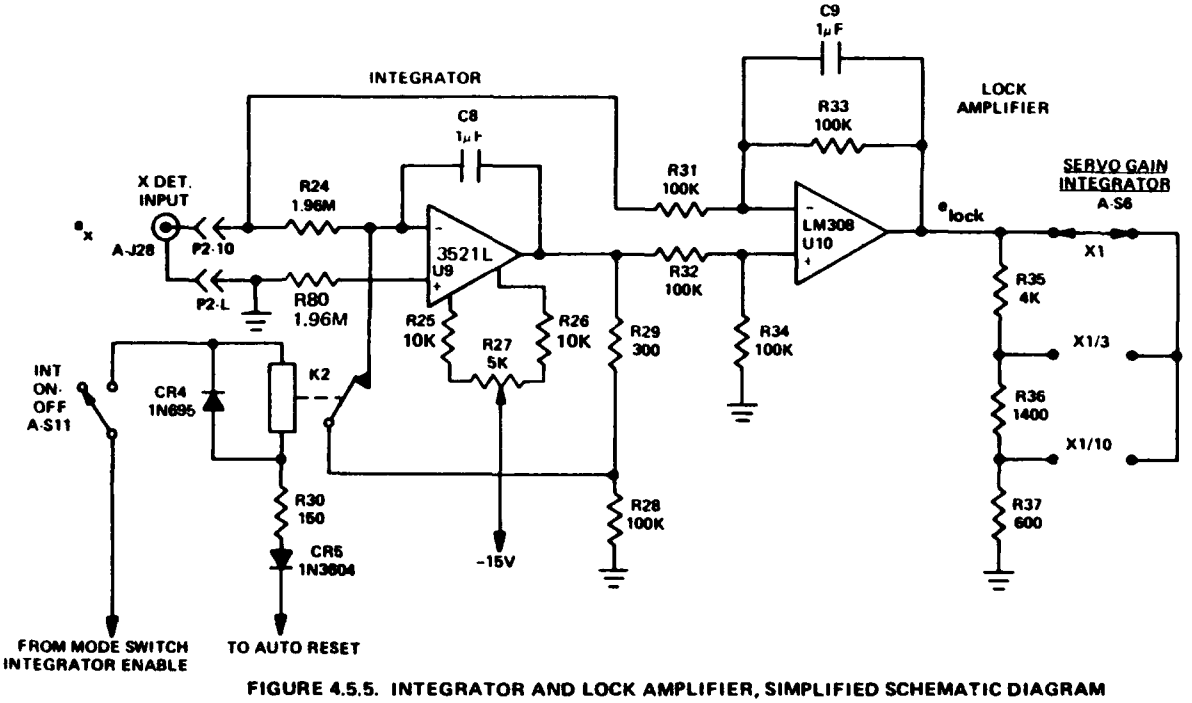


FIGURE 4.5.5. INTEGRATOR AND LOCK AMPLIFIER, SIMPLIFIED SCHEMATIC DIAGRAM

The first term is the responses of the lock amplifier, giving unity gain with a lag break at 0.1 sec. The second term is the response of the integrator with its time constant of 2 seconds. It is the function of the integrator to provide very high dc gain to null the reactive unbalance of the bridge by servoing the synthesizer.

To avoid errors in the balance point of the "X" det (reactive component), the integrator must be free of dc offset, drift and have very high dc gain. As discussed in section 4.5.2, the integrator errors due to op amp limitations are:

$$e_{error} = \frac{1}{R24\ C8}\int_0^t \frac{e_o}{A}\,dt + \frac{1}{R24C\ C8}\int_0^t V_{os}\,dt + \frac{1}{C8}\int_0^t i_b\,dt + \frac{e_o}{A} + V_{os}$$

The critical term is the second one where a V_{os} of less than 67uV is required to keep the integrator from drifting more than one millivolt in 30 seconds. By using a hybrid FET input op amp and trimming the offset voltage, this requirement can be met over a modest temperature range. Trimming to less than 25uV is possible at any given temperature. To meet the 1 mV drift in 30 second drift rate, readjustment may have to be done if the ambient temperature changes by more than 20^{o}C. An internal adjustment (R27) is provided. The Burr-Brown 3521L hybrid op amp U9 used here has the necessary gain, low bias current and provision for trimming the offset voltage.

The integrator is enabled only when INT switch A-S11 is ON and MODE switch A-S9 is in LOCK or AUTO position. In the AUTO mode the integrator remains reset (OFF) until the crystal response is detected and contacts 2 and 7 of relay K1 ground the return side of relay K2's coil through diode CR5. This eliminates integrator response to signals until the sweep is stopped.

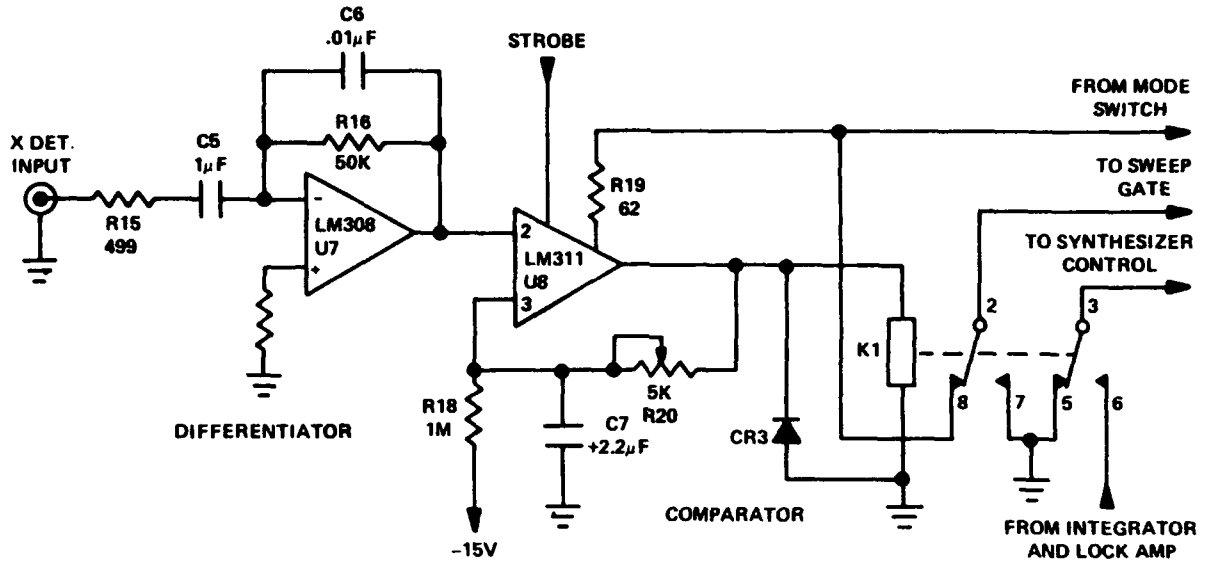


FIGURE 4.5.6.1. DIFFERENTIATOR AND COMPARATOR, SIMPLIFIED SCHEMATIC DIAGRAM

4.5.6 Differentiator and Comparator

The automatic acquisition of lock requires a detector to stop the sweep at the lowest frequency crystal response. This consists of a differentiator and an adjustable threshold comparator shown in Figure 4.5.6.1.

The differentiating is done at low frequency where the response is controlled by R16 and C5. Here the output voltage is given by:

$$E_{out} = R16\ C5\ \frac{dE_{in}}{dt}$$

To eliminate the response to low amplitude high frequency noise, R15 and C6 are added to reduce the high frequency gain beginning at $\omega = \frac{1}{R15\ C5} = \frac{1}{R16\ C6} = 2000$ or 318 Hz. The measured gain of the complete differentiator is shown in figure 4.5.6.2.

The output of the differentiator drives a voltage comparator arranged with positive feedback to act as a latch when the preset threshold

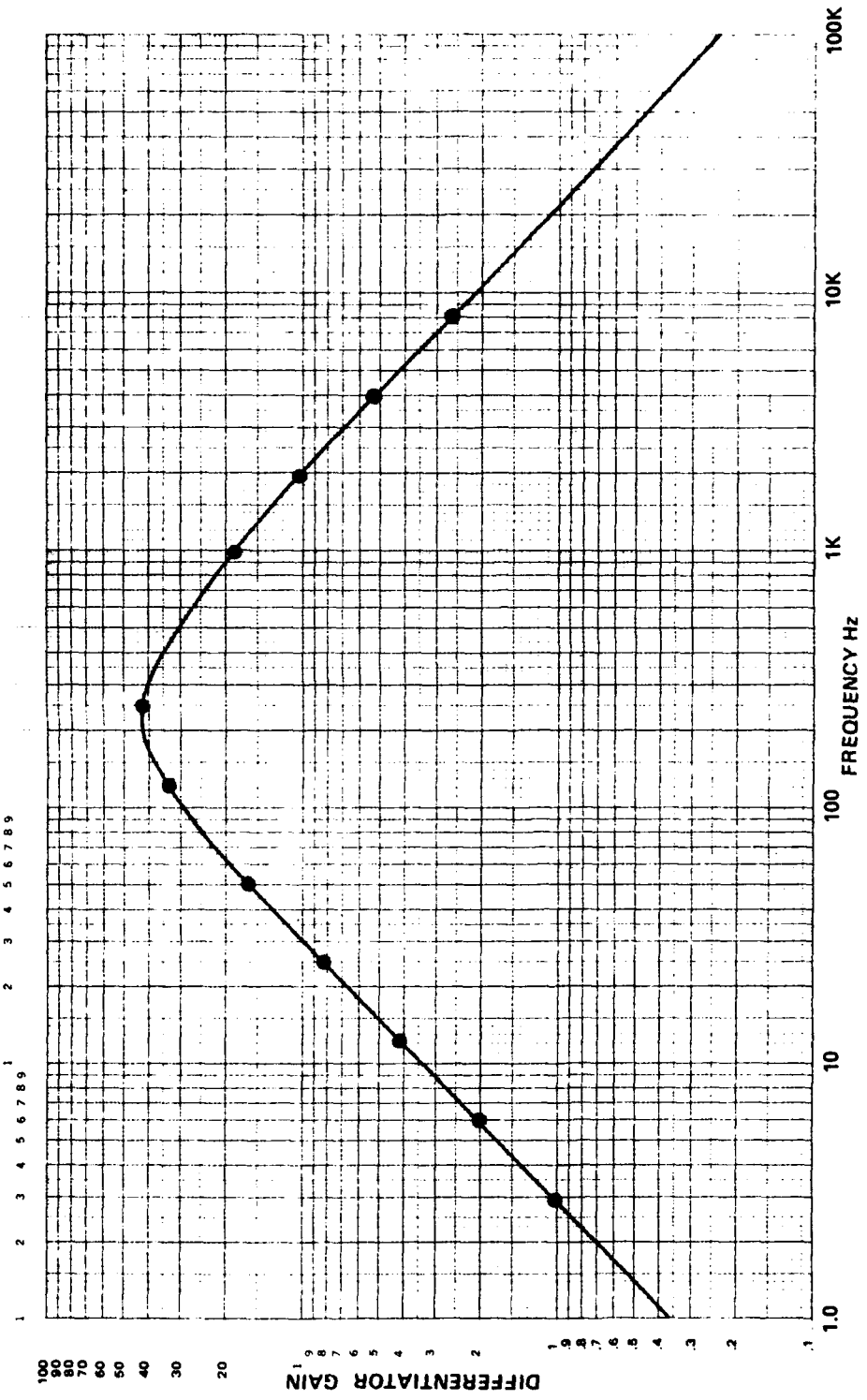


FIGURE 4.5.6.2. DIFFERENTIATOR GAIN VS FREQUENCY CURVE

is exceeded. The threshold is internally adjustable with the 5K potentiometer R20 from 0 volts to -75mV. This allows a comparator threshold setting corresponding to input voltage changes from nearly 0 to 1.5 V/sec. Any signal within the bandwidth of the differentiator that exceeds this preset rate of change will energize relay K1 at the comparator output. This relay in turn, (1) stops the sweep by grounding an input to the NAND gate U2A driving the CMOS counter of the sweep generator, (2) turns on the integrator (if it is not manually turned off) by connecting a dc return for its ON/OFF relay K2 and (3) connects the lock signal to the synthesizer amplifiers. These operations complete the automatic search and lock function.

A delay output timer U11 provides a delayed contact closure to ground after completion of the search and lock. The contact closure is available on two pins (C and D) of the REMOTE connector A-J24 on the rear panel. The delay time is adjustable by a 10M rear panel screw control A-R20 from less than 1 second to greater than 100 seconds. The delay timer along with the search and lock gates are shown in figure 4.5.6.3.

The delay timer uses a LM322 Precision Timer which is capable of long timing periods. The 10uF timing capacitor C4 is a low leakage wet-slug tantalum electrolytic. A 100-ohm resistor R13 in series allows the timer to be reset before completion of the timing interval if SEARCH pushbutton A-S8 is depressed.

By pushing the SEARCH button, the 2.2 uF capacitor C3 is charged through resistor R12, raising the voltage at the input to the delay timer sufficiently to cause U11 to reset. Grounding the input to the first NAND gate through these resistors drives its output high which resets the sweep

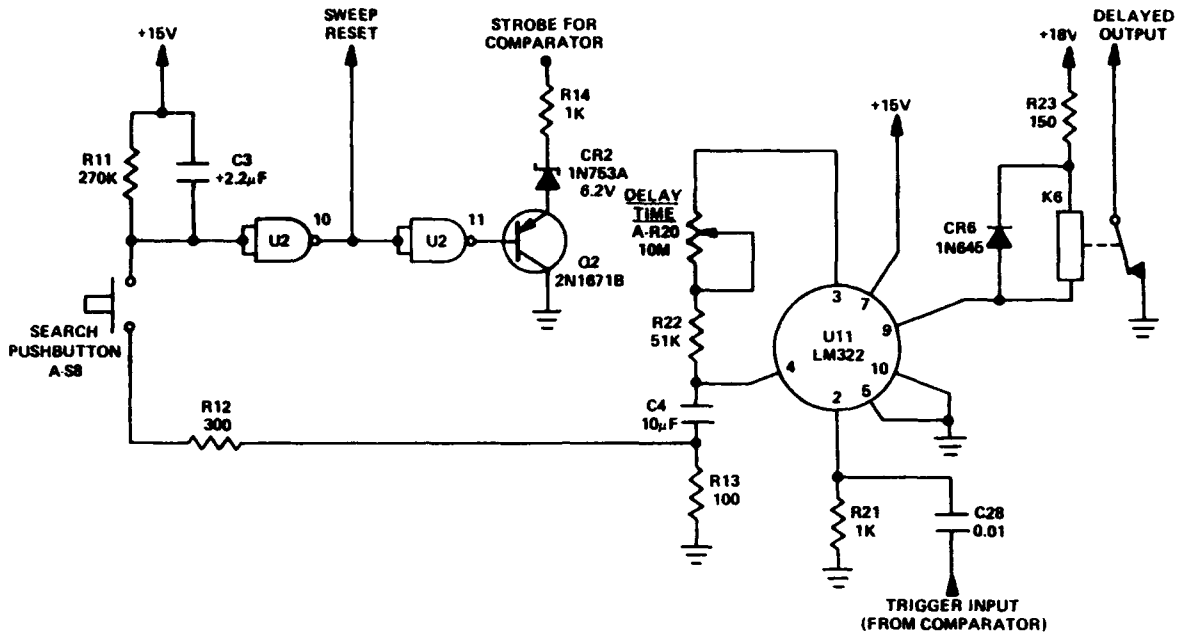


FIGURE 4.5.6.3. DELAY TIMER, SEARCH & LOCK GATES, SIMPLIFIED SCHEMATIC DIAGRAM

counter. As C3 discharges through resistor R11, the NAND gate thresholds are reached. The first gate releases the sweep counter reset. The second gate, also used as an inverter, arms the comparator by drawing current from the strobe terminal. The delay introduced by the 2.2 uF capacitor and 270K resistor (about 1/2 second) allows the sweep to be reset to the voltage corresponding to the lowest frequency and all associated transients to die out before the sweep is started and the comparator is armed.

4.5.7 RF Meter Amplifier

A front panel meter A-M4 is used to monitor the output power from the RF power amplifier. In addition, red sectors at each end of the meter scale are used as out of range indicators for the ALC. The meter amplifier and ALC limit comparators are shown in figure 4.5.7.

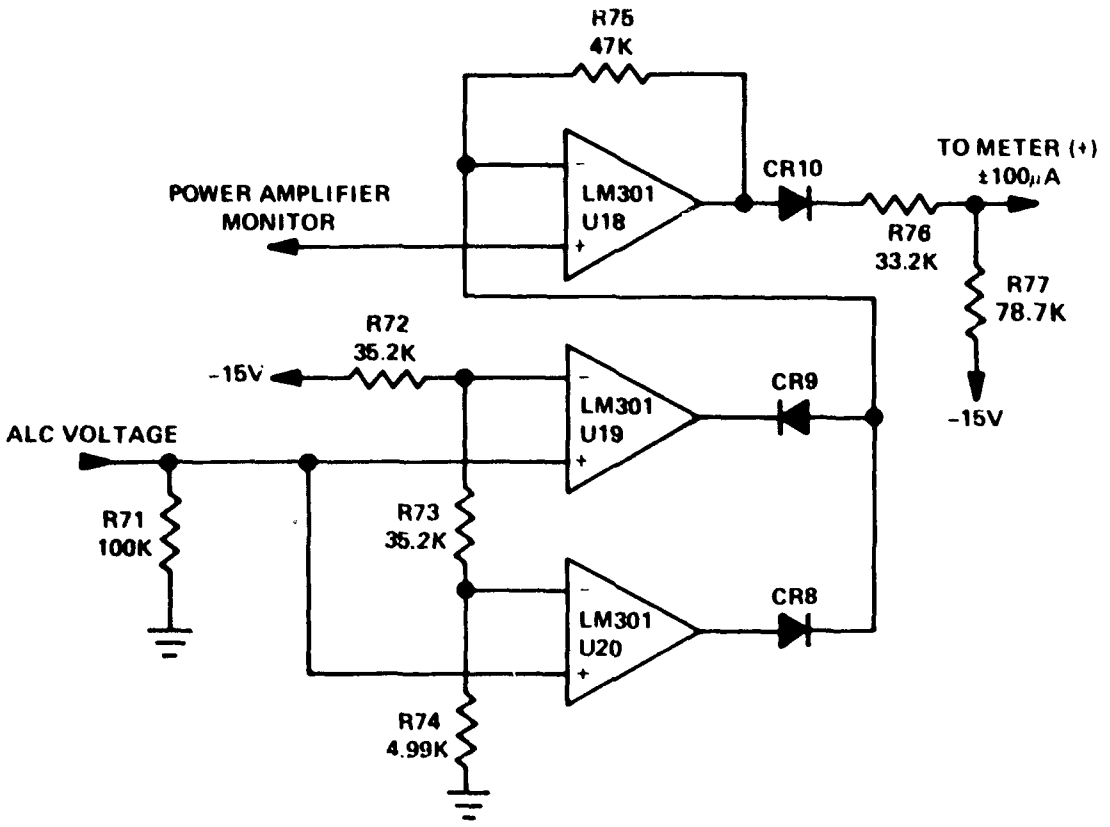


FIGURE 4.6.7. METER AMPLIFIER AND ALC LIMIT COMPARATORS, SIMPLIFIED SCHEMATIC DIAGRAM

Amplifier U18 is a voltage follower which provides the meter drive current. Calibrating the meter at the required +30 dBm point is done by varying either the current to the meter by changing resistor R76 or the dc offset by changing resistor R77. Meter accuracy over the full +24 to +30 dBm range is ±1/2 dB.

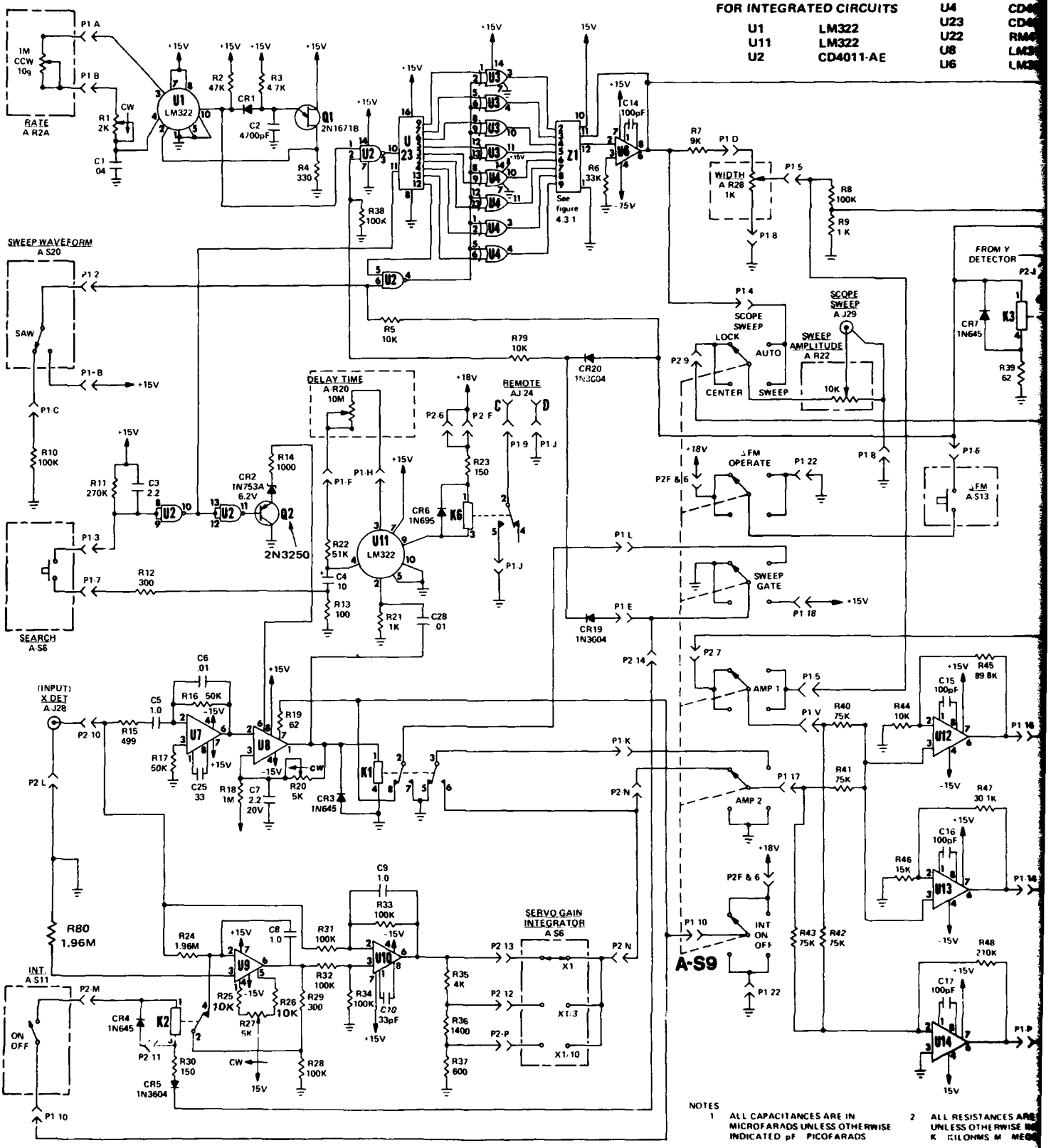
Op amps U19 and U20 are used as comparators. One is biased at nearly the upper limit of the ALC. The other is biased at nearly the lower limit of the ALC. When the ALC voltage is more positive than the threshold of op amp U20, this op amp is driven against its upper stop. This causes the meter amplifier to swing to the negative stop, driving the meter into the lower red sector labled "LO". This indicates that the generator drive signal is too low

and beyond the ALC range. Likewise when the ALC voltage is more negative than the threshold of the op amp U19, it goes against the negative stop. This in turn drives the meter amplifier and the meter to the upper stop. The red sector of the meter here is labeled "HI" indicating that the generator drive signal is too high for the ALC range. The diodes (CR9 and CR8) at the outputs provide proper steering of the comparator signals. Sufficient margin in the ALC limit setting assures proper operation when the meter is not in a red sector.

Operation when the ALC indicates that the input generator input is too high will result in distortion at the output. When the ALC indicates that the generator input is too low, the output will not be leveled.

4.5.8 Complete Circuit

Schematic diagrams of the complete Sweep & Servo Amplifier are shown in Figures 4.5.8.1 through 4.5.8.3.



U3	CD4030-AE	U7	LM308	U16	LM308
U4	CD4030-AE	U10	LM308	U17	LM308
U23	CD4040-AE	U12	LM308	U18	LM308
U22	RM4195-T	U13	LM308	U9	3521L
U8	LM311	U14	LM308	U19	LM301A
U6	LM308	U15	LM308	U20	LM301A

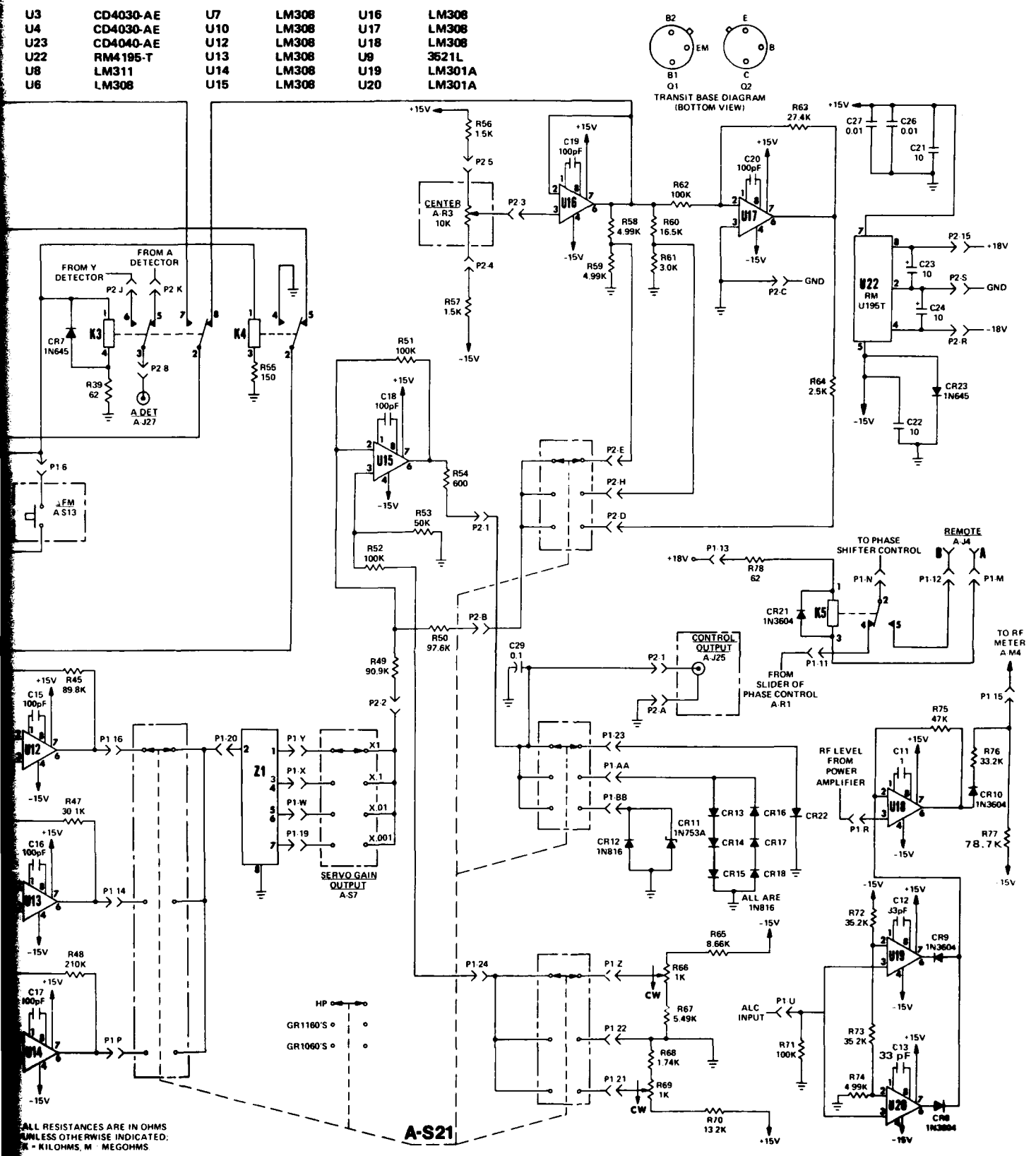


FIGURE 4.5.8.1. SERVO/SWEEP MODULE, SCHEMATIC DIAGRAM

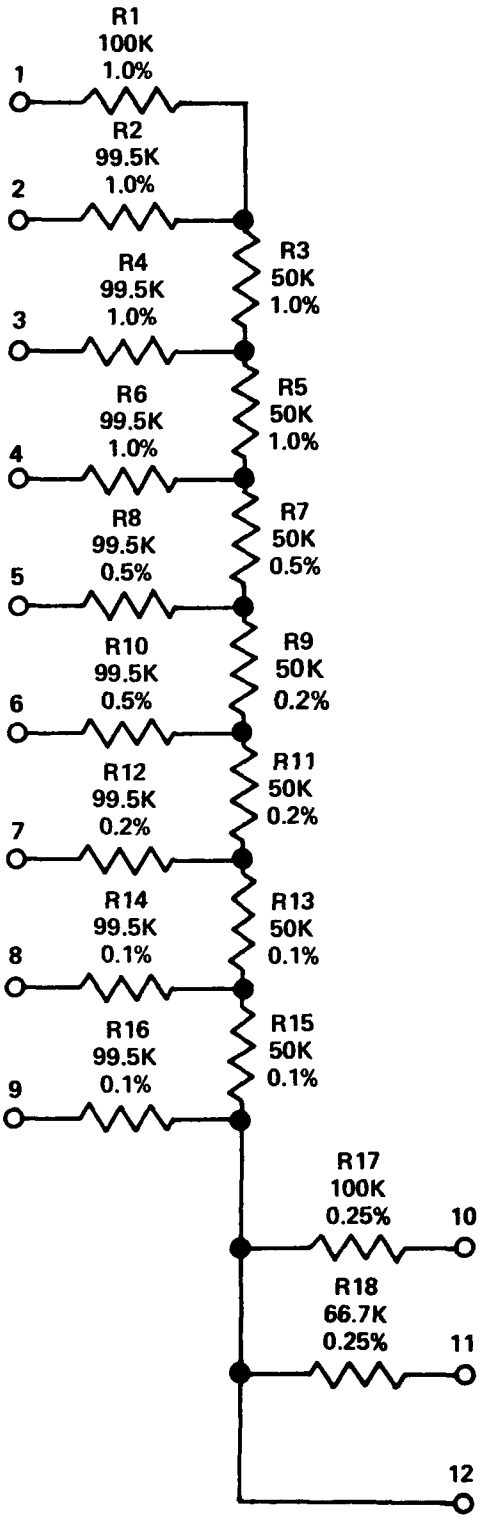


FIGURE 4.5.8.2. THIN-FILM RESISTOR NETWORK INTEGRATED CIRCUIT Z1, SCHEMATIC DIAGRAM

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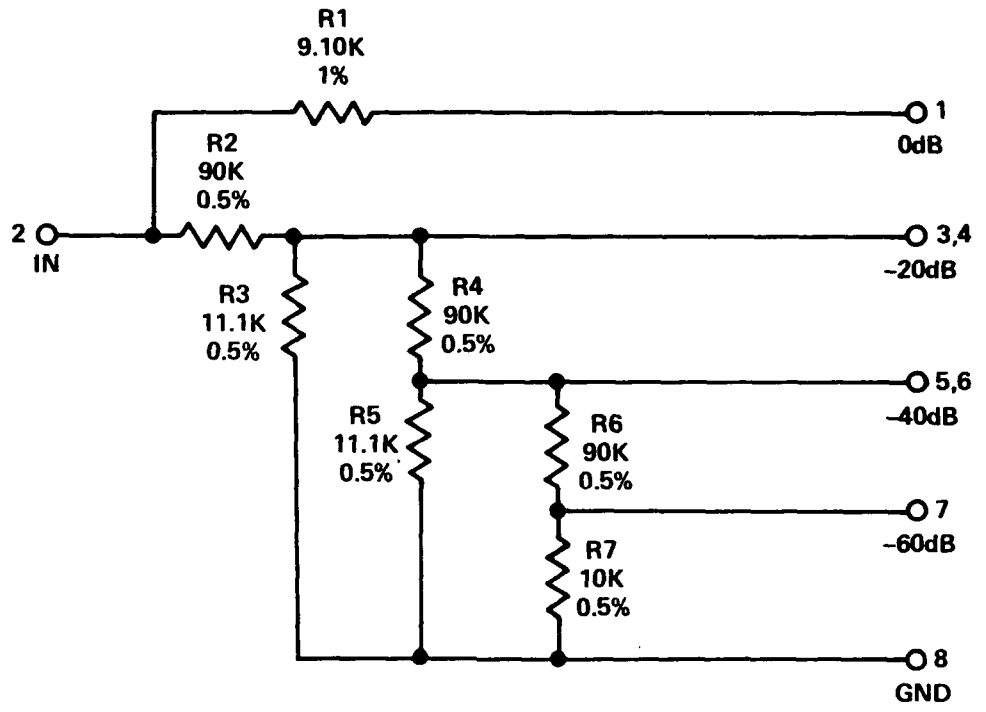


FIGURE 4.5.8.3. THIN-FILM RESISTOR NETWORK INTEGRATED CIRCUIT Z2, SCHEMATIC DIAGRAM

4.6 IF Reference and Phase Shifter

4.6.1 General

The 80-kHz IF signal from the Reference Mixer is processed by this module to provide synchronous detector reference signals which are continuously adjustable in phase over 360^{o}. A dc signal controls the phase shift and remote programming is possible.

The phase shifter is a phase lock-loop that permits the user to establish any desired phase relation between the reference signal and the oscillator output. Figure 4.6.1 shows the basic arrangement. The reference input and the output from the voltage-controlled oscillator (VCO) are compared in the phase detector (Ø) which produces a dc output E_1 proportional to the phase difference between them. E_2 is the dc phase control voltage. The ampli-

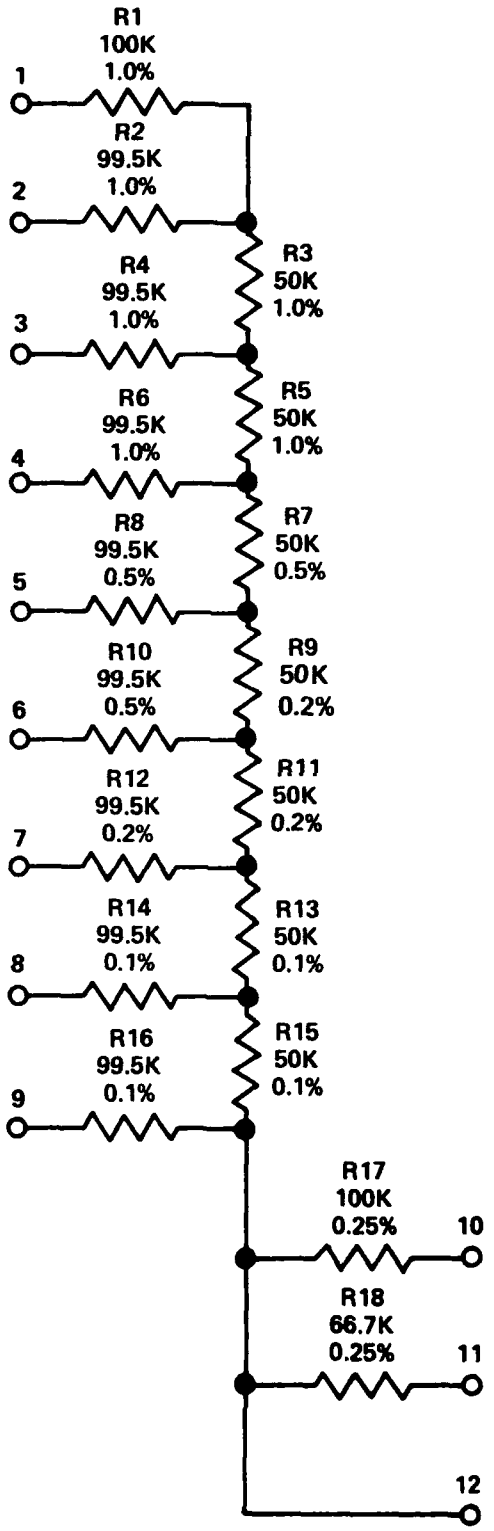


FIGURE 4.5.8.2. THIN-FILM RESISTOR NETWORK INTEGRATED CIRCUIT Z1, SCHEMATIC DIAGRAM

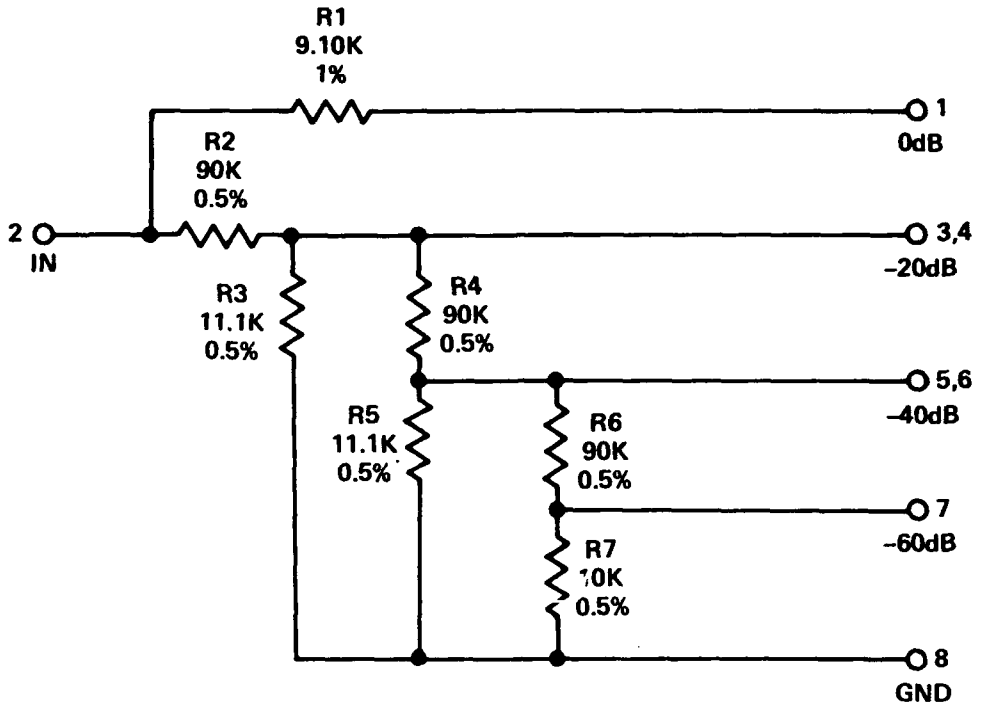


FIGURE 4.5.8.3. THIN-FILM RESISTOR NETWORK INTEGRATED CIRCUIT Z2, SCHEMATIC DIAGRAM

4.6 IF Reference and Phase Shifter

4.6.1 General

The 80-kHz IF signal from the Reference Mixer is processed by this module to provide synchronous detector reference signals which are continuously adjustable in phase over 360^{o}. A dc signal controls the phase shift and remote programming is possible.

The phase shifter is a phase lock-loop that permits the user to establish any desired phase relation between the reference signal and the oscillator output. Figure 4.6.1 shows the basic arrangement. The reference input and the output from the voltage-controlled oscillator (VCO) are compared in the phase detector (Ø) which produces a dc output E_1 proportional to the phase difference between them. E_2 is the dc phase control voltage. The ampli-

fier (A) has large dc gain which forces E_1 to equal E_2. Since E_1 is proportional to the phase difference, so is the dc programming voltage E_2. Very good linearity can be obtained and, if a potentiometer of adequate linearity is used, better than 1^o accuracy is obtained.

4.6.2 Reference IF

The IF signal from the reference mixer is fed to a single tuned circuit with a bandwidth of 1.5 kHz. A digital comparator provides a square-wave signal of nearly B+ amplitude to drive the digital circuitry of the phase shifter. Figure 4.6.2 shows the circuit. An IF input signal of about 0.5 mV rms is sufficient but the typical level is 15 mV rms.

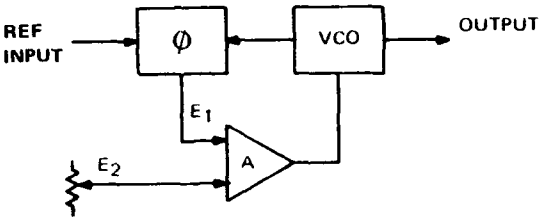


FIGURE 4.6.1. BASIC PHASE SHIFTER CIRCUIT, BLOCK DIAGRAM

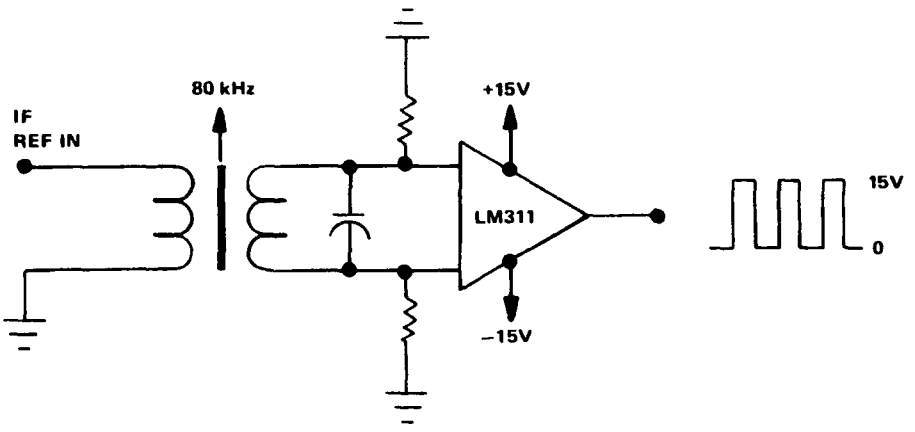


FIGURE 4.6.2. DIGITAL COMPARATOR CIRCUIT

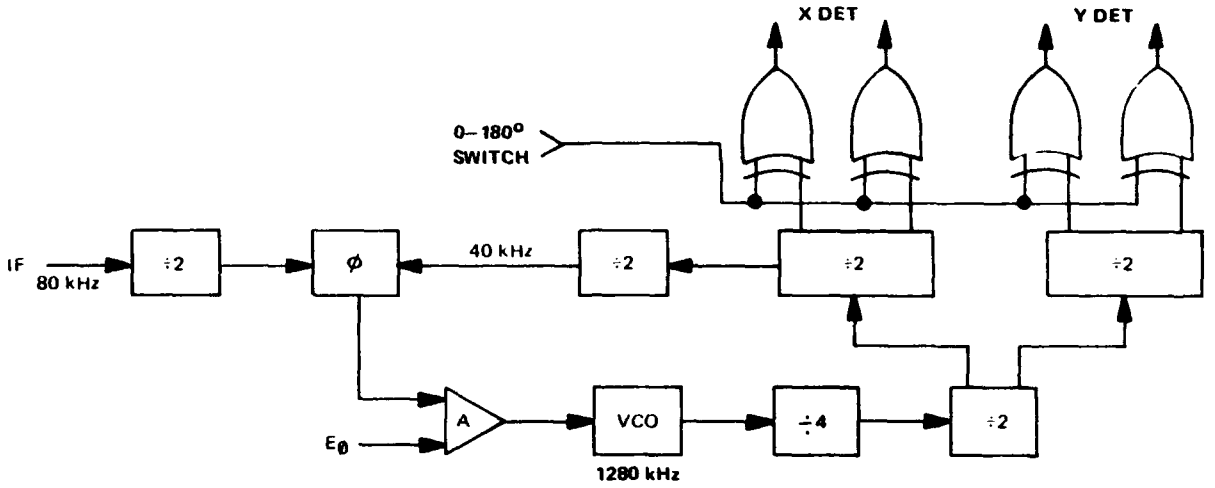


FIGURE 4.6.3.1. PHASE SHIFTER

4.6.3 Phase Shifter

The basic circuit as shown in Figure 4.6.1 has several limitations. The phase-detector is a flip-flop which is "set" by one of the signals and "reset" by the other. The pulse-pair resolution is limited and as a result it does not function near zero or 360° phase difference.

The full 360° range is covered by dividing both of the 80-kHz signals down to 40 kHz. The phase detector will then easily handle the full 360° (at 80-kHz), as this corresponds to only half the theoretical capability at 40 kHz. By proper choice of circuitry, the 0-360° phase difference at 80 kHz is made to correspond to 90° to 270° at the 40 kHz phase detector. This not only provides more than 360° capability but also improves the linearity of the programming.

Four reference signals precisely 90° apart are needed at 80 kHz for the switching type synchronous detectors. These signals can be generated with digital accuracy by running the VCO in the lock-loop at a frequency at least 4 times 80 kHz. The arrangement of the phase-shifter circuitry is shown in

Figure 4.6.3.1. The VCO runs at 1280 kHz. A series of flip-flops divides the VCO signal and generates the drive signals for the X and Y detectors.

Four exclusive or gates are included to provide a convenient way to shift the reference phase by exactly 180°. Operated by a front panel switch, this feature is useful for the servo lock-up procedure. This 180° phase shift is accurate to about 0.1 degree.

The external phase programming requires a dc voltage from approximately +3 to +11 V.

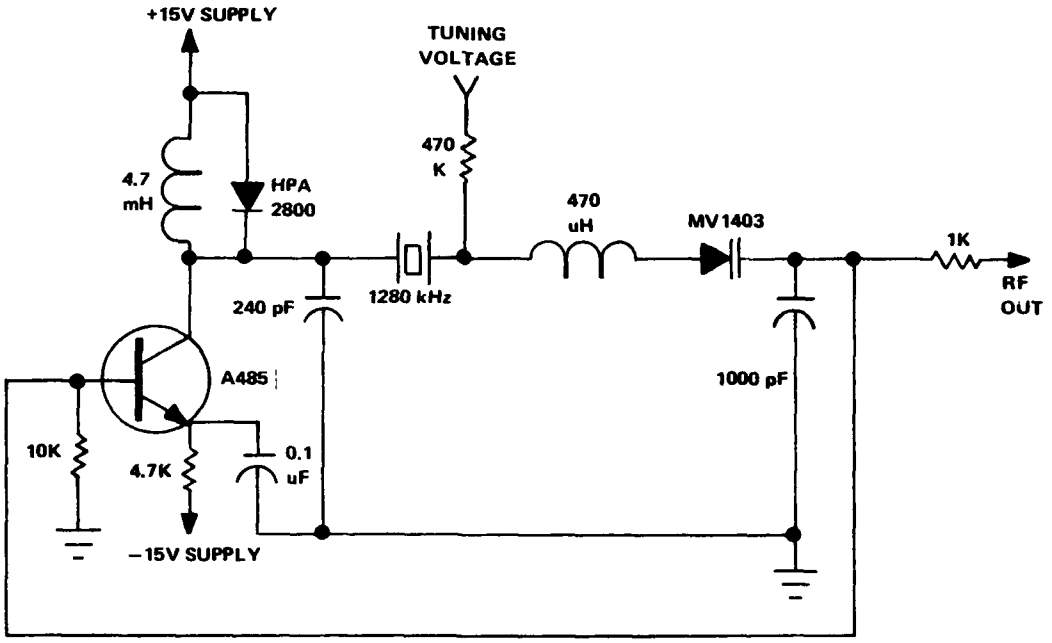


FIGURE 4.6.4. VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR, SCHEMATIC DIAGRAM

4.6.4 VCXO

The reference IF signals are derived from a voltage controlled cyrstal oscillator (VCXO) operating at 1280 kHz. The use of a crystal oscillator permits a lock-loop with very high dc gain, reducing the static error coefficient to less than 0.5 degree for the full lock range. This results in

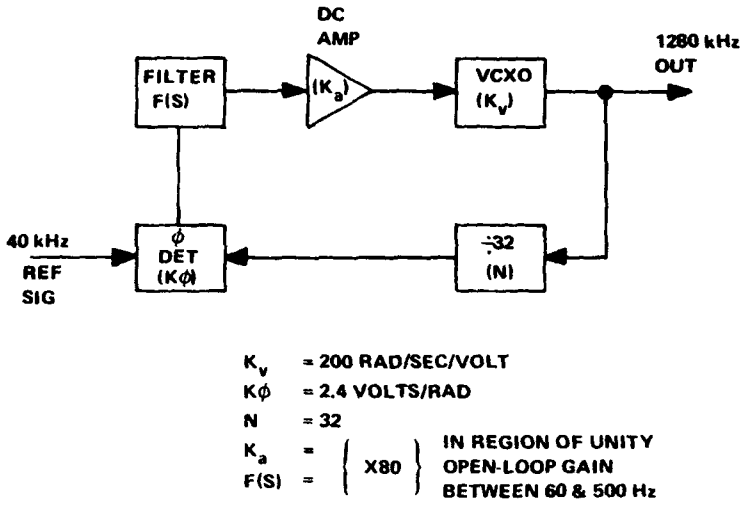


FIGURE 4.6.5.1. IF REFERENCE OSCILLATOR LOCK LOOP, BLOCK DIAGRAM

high phase-shifter accuracy, better than 0.5 degree for external dc programming and better than 2 degrees from the front panel control where the accuracy is reduced because of potentiometer non-linearity.

The quartz crystal is tightly specified for inductance and temperature coefficient to insure a lock range of ±50 ppm under all operating conditions.

The oscillator circuit is conventional and is shown in Figure 4.6.4. It is a pi-network configuration with the crystal operating around series resonance as determined by the reactance of the hyperabrupt varactor diode. The average tuning sensitivity is 200 radians/sec/volt.

4.6.5 Lock Loop

The IF reference oscillator lock loop contains the basic blocks shown in Figure 4.6.5.1. The set-reset flip-flop phase detector provides an output of 2.4 volts/radian. It is followed by a second-order RC active filter having a 1600 Hz cutoff frequency. A main loop amplifier provides high dc gain

and a controlled roll off characteristic as required for servo lock-up and stability. A resistive network translates the ±15 volt loop amplifier output to the -2 to -10 volt range required by the VCXO.

A plot of the open-loop frequency response characteristic of the complete lock loop is shown in Figure 4.6.5.2.

4.6.6 Test & Performance Data

A schematic diagram of the complete IF Reference and Phase Shifter module is shown in Figure 4.6.6. The performance of the module has been satisfactory in all respects.

All 1280 kHz quarts crystals used in the production lot were measured for temperature coefficient and pulling range. A lock range of ±50 ppm is easily ensured under all conditions.

The IF reference signal drive margin was at least 25 dB for all units.

4.7 Synchronous Detectors

4.7.1 General

Switching type synchronous detectors are used for the X and Y detectors. These circuits offer better performance and require less critical adjustment than analog type detectors. They also interface more easily with the digital reference signals.

4.7.2 Input Buffers

The 80 kHz signal from the IF amplifier is buffered by LM310 integrated circuit voltage followers ahead of each synronous detector. These circuits

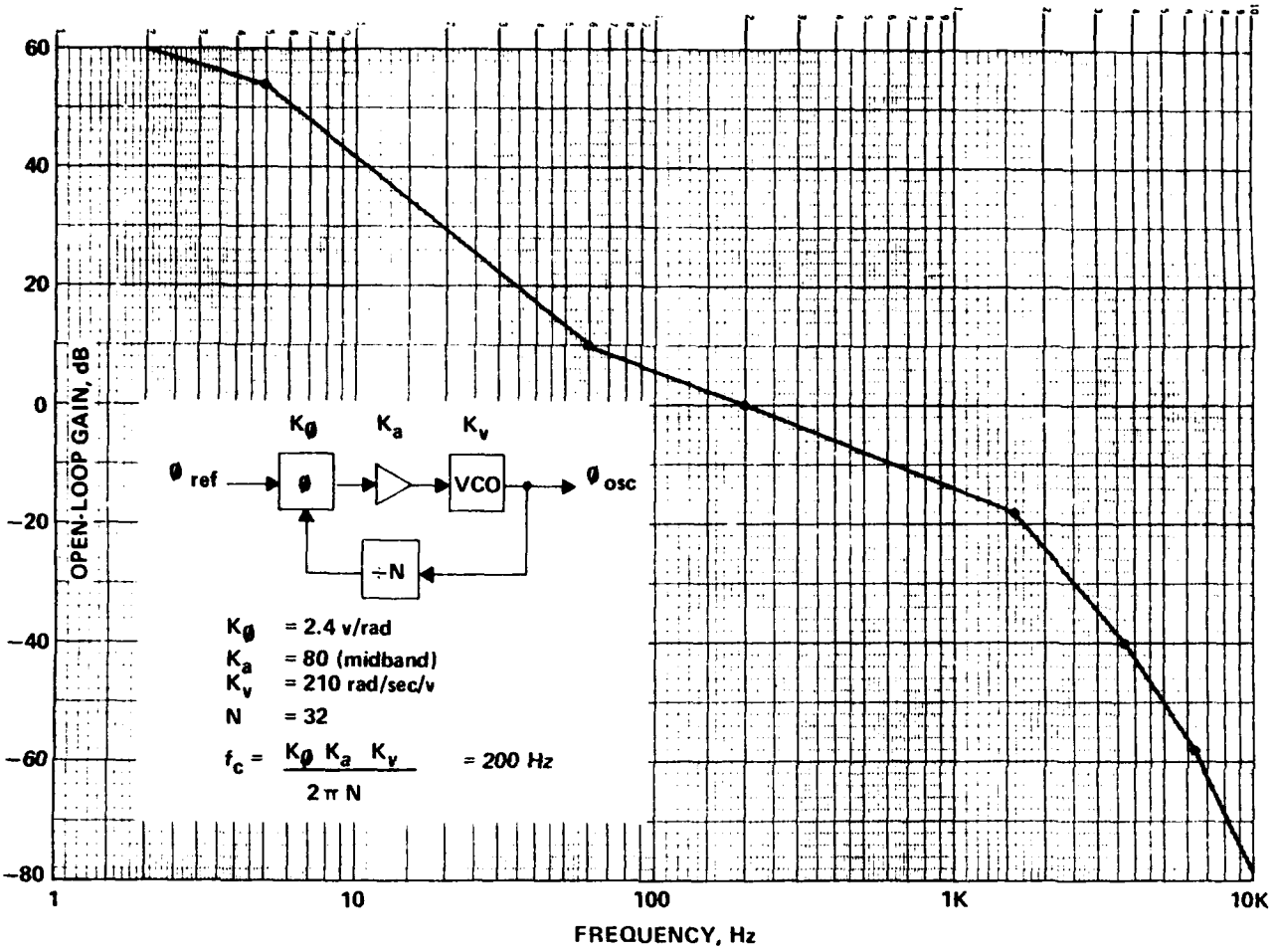


FIGURE 4.6.5.2. IF REFERENCE OSCILLATOR LOCK LOOP, OPEN-LOOP FREQUENCY RESPONSE

provide isolation between the two channels. Two back-to-back Zener diodes are provided to shunt an excessive input signal to ground.

4.7.3 Synchronous Detector Analysis

The basic synchronous detector circuit is shown in Figure 4.7.3.1. FET switches connect the circuit in such a way that, for one half-cycle of the reference signal, the op amp is in the inverting mode and for the other half-cycle in the noninverting mode. The output is a full-wave rectified signal. The same op amp provides integration of this waveform so that the output is dc with low ripple.

In order to have equal gain for the two half-cycles, the following condition must be met:

$$R_6 = \frac{(R_1 + R_3)\, R_3\, R_5}{(R_1 + R_5)\,(R_3 + R_5) - R_3\, R_5} \qquad \begin{matrix} R_1 = R_2 \\ R_3 = R_4 \end{matrix}$$

The stage gain is:

$$A = \frac{R_5}{R_1 + R_3}$$

The dc output voltage is:

$$E_{dc} = \frac{A}{\pi} \int_0^{\pi} E_p \sin\theta \; d\theta = \frac{2A\, E_p}{\pi}$$

where A is the stage gain.

E_p is the peak ac applied.

For a stage gain of A = 1

$$E_{dc} = 0.637\, E_{peak} = 0.900\, E_{rms}$$

The resistor networks R1 through R6 are thin-film type to provide good tracking and accuracy. The FET switches have to be selected for use as matched pairs for smallest change in dc output when the reference drive is applied in the absence of an IF signal. Small trimmer capacitors permit final precise capacitive balance. The result is that the change in dc output from no reference signal to the full 15-V peak-to-peak reference signal can be adjusted be be zero and long-term stability should be adequate.

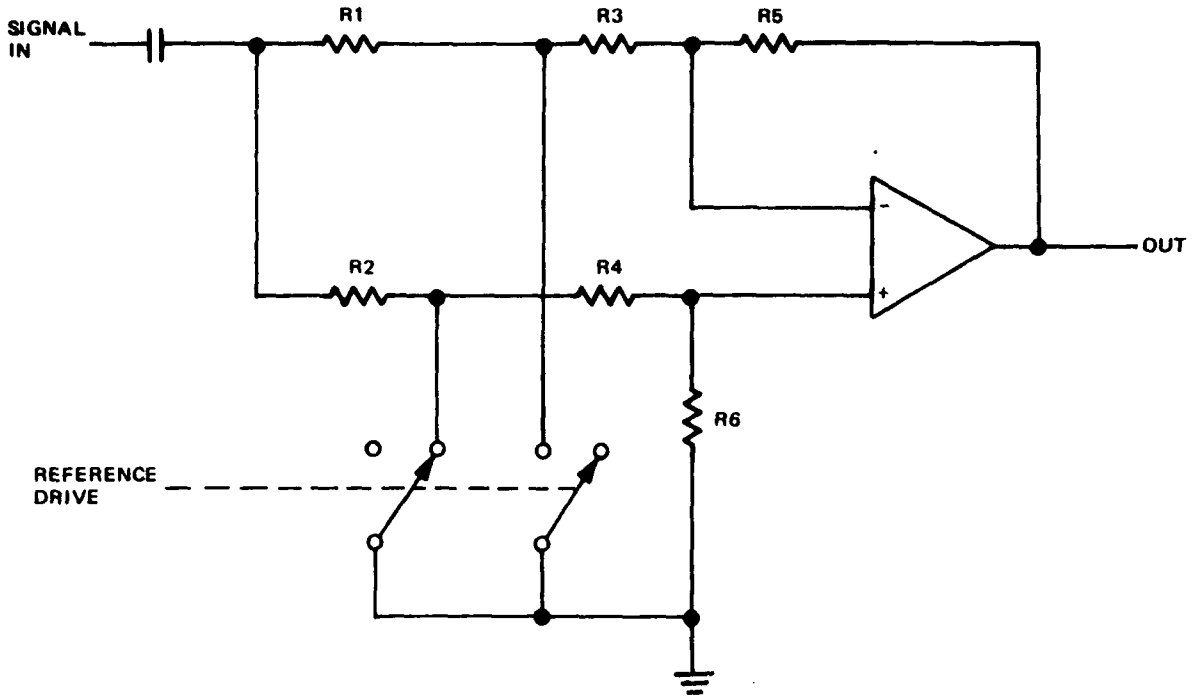


FIGURE 4.7.3.1. BASIC SYNCHRONOUS DETECTOR, SIMPLIFIED SCHEMATIC DIAGRAM

The op amp must have good long-term stability of the offset voltage and very high input impedance. A Burr-Brown 3521L hybrid FET op amp was chosen because of excellent overall characteristics.

The complete circuit schematic is shown in Figure 4.7.3.2.

4.7.4 Test & Performance Data

The performance of the synchronous detectors is excellent. The quadrature rejection is greater than 80 db and is limited by the ability to set the reference phase. The dc offset of the detectors can be trimmed to under 25 uV and has a temperature coefficient of only 1 uV/^{o}C. The drive offset is adjustable to under 20 uV. The 180^{o} phase reversal offset is a function of the reference drive symmetry and is kept below 30 uV for the critical X detector by device selection.

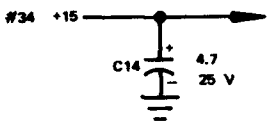
INTEGRATED CIRCUITS

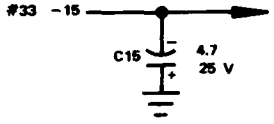
REFERENCE DESIGNATORS

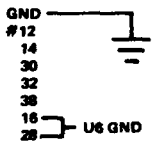
U1, 9	LM311
U2-5	INS4013S
U6	INS4030S
U7	LM310
U8	LM301A

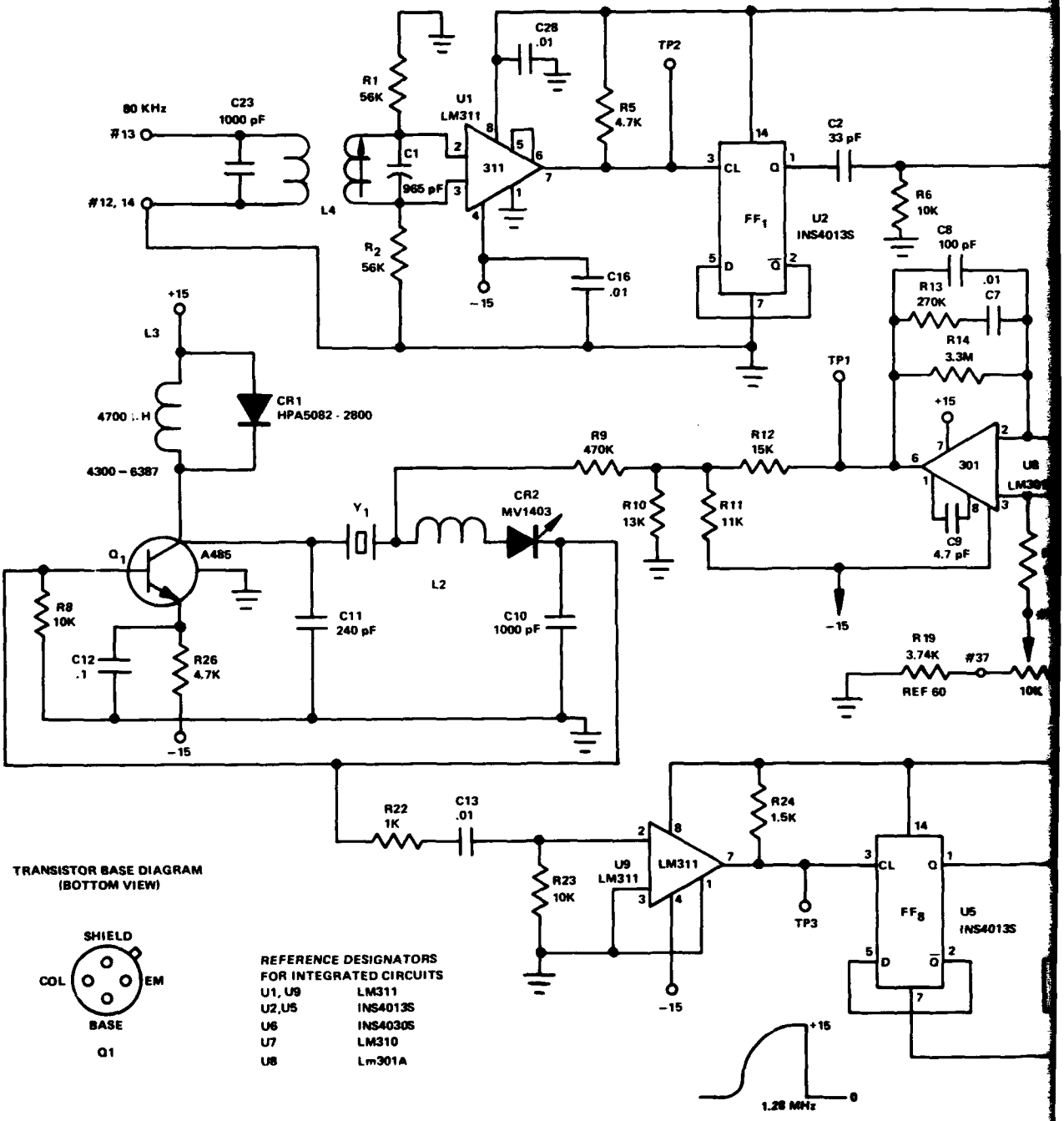
COMPONENT NUMBERS USED:

R1, R2, R5 – R27
C1, C28
Q1
Y1
U1 – U9
L2, L3, L4
CR1, CR2









TRANSISTOR BASE DIAGRAM
(BOTTOM VIEW)

Q1

REFERENCE DESIGNATORS FOR INTEGRATED CIRCUITS

U1, U9	LM311
U2,U5	INS4013S
U6	INS4030S
U7	LM310
U8	Lm301A

DC POWER +15 20 mA
–15 17 mA

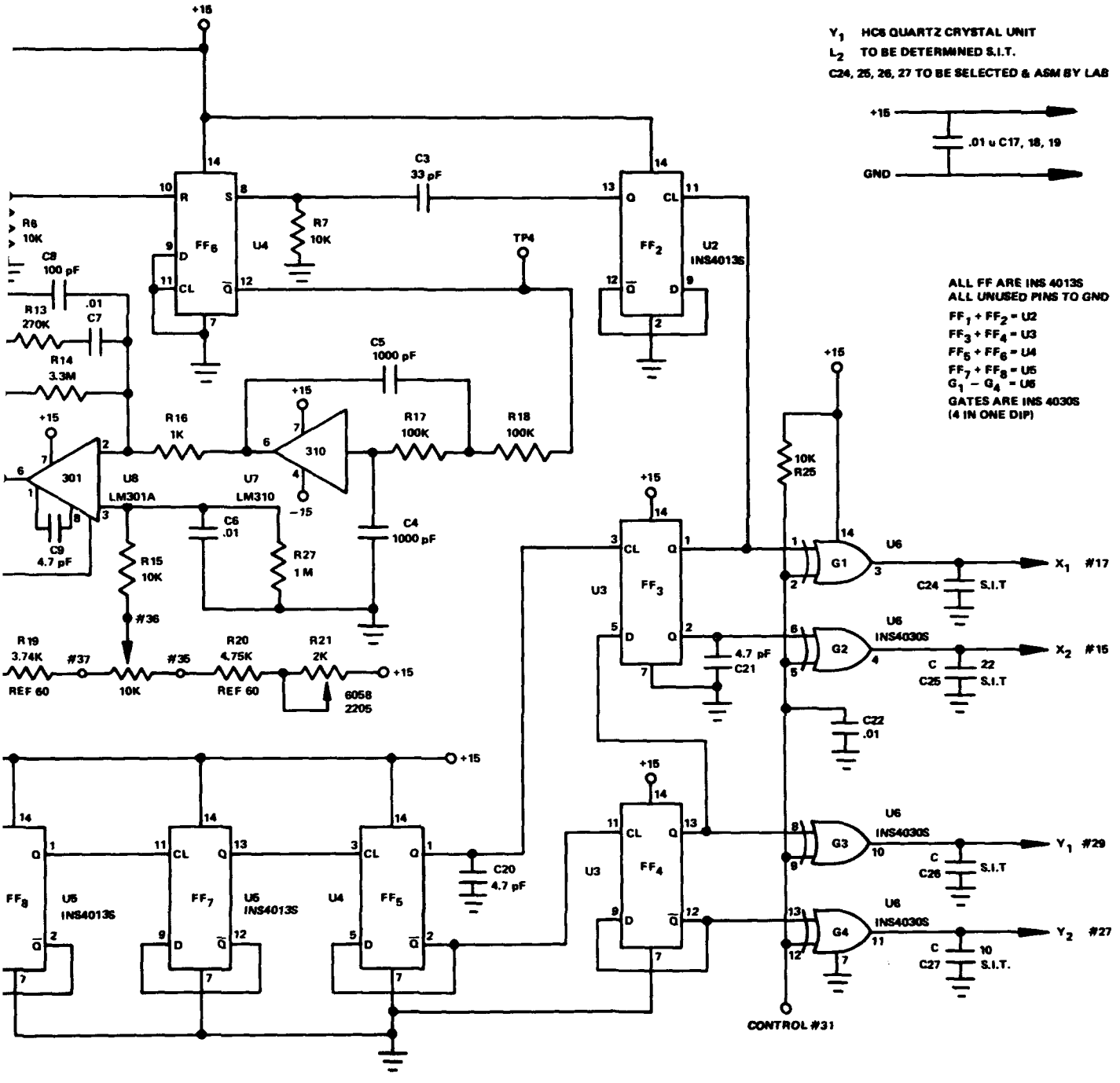


FIGURE 4.6.6. IF REFERENCE AND PHASE SHIFTER MODULE, SCHEMATIC DIAGRAM

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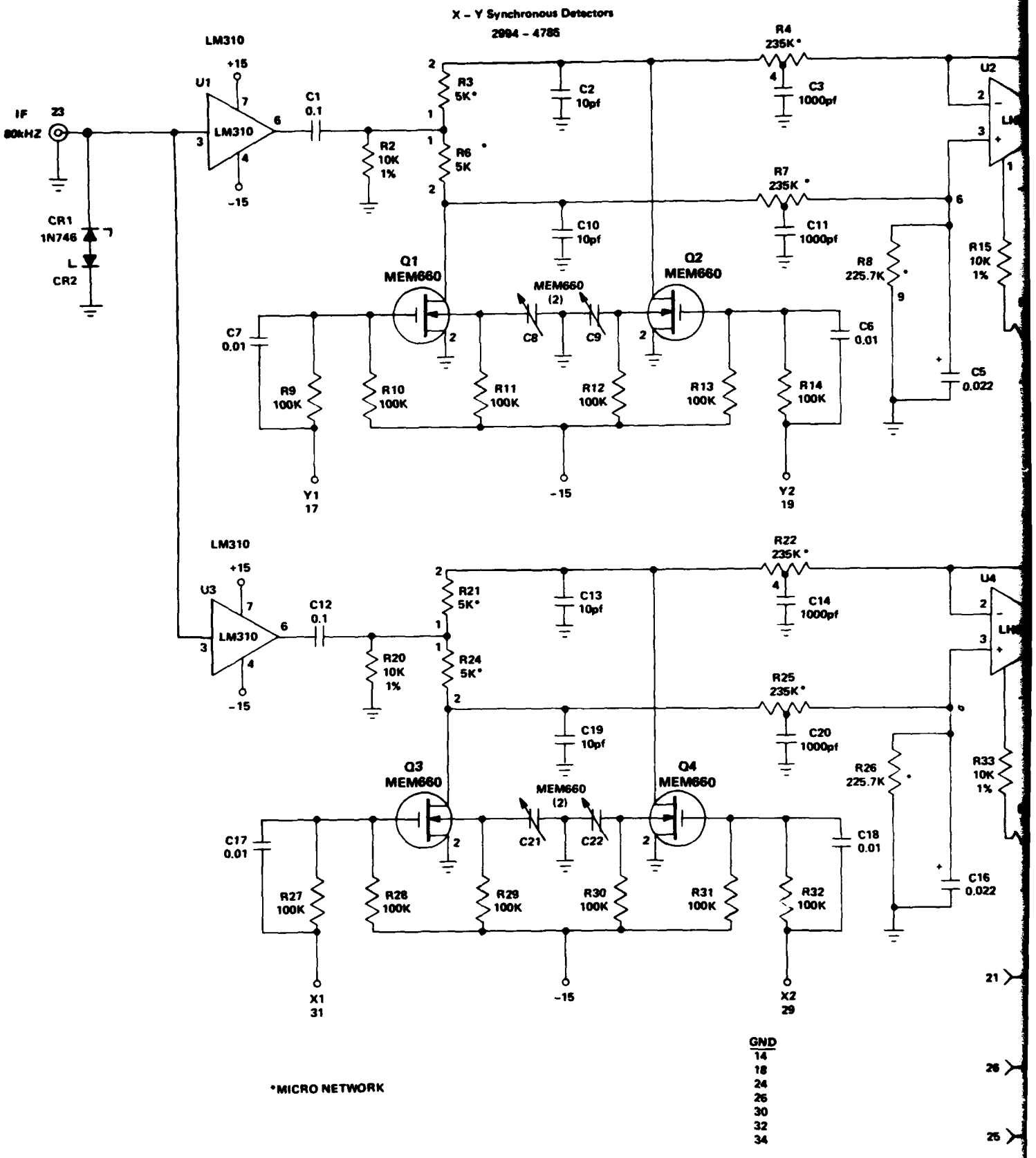


FIGURE 4.7.3.2. X AND Y SY

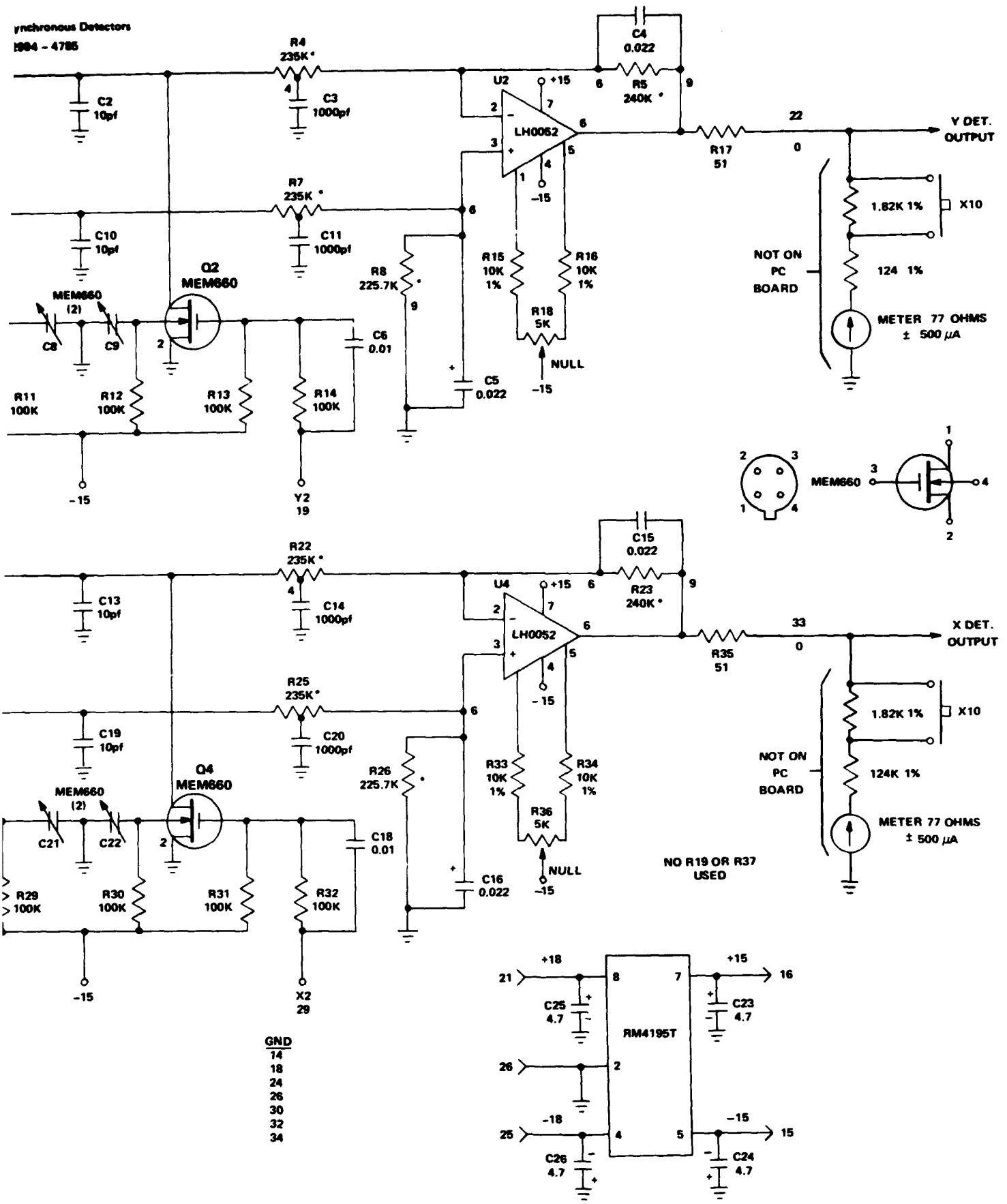


FIGURE 4.7.3.2. X AND Y SYNCHRONOUS DETECTORS, SCHEMATIC DIAGRAM

4.8 Isolation Modules

4.8.1 Introduction

Isolation Modules for the Generator and LO signals are vital elements of this instrument if the detectivity is not to be limited by the presence of spurious leakage signals.

A block diagram of the basic receiver is shown in Figure 4.8.1.1. There are two separate signal paths, one through the crystal bridge and the other serving to produce a reference signal for the synchronous detectors. The isolation modules not only split the generator and LO inputs into these paths but also keep them isolated. In particular it is vital to prevent leakage of generator signal into the receiver input via the LO path.

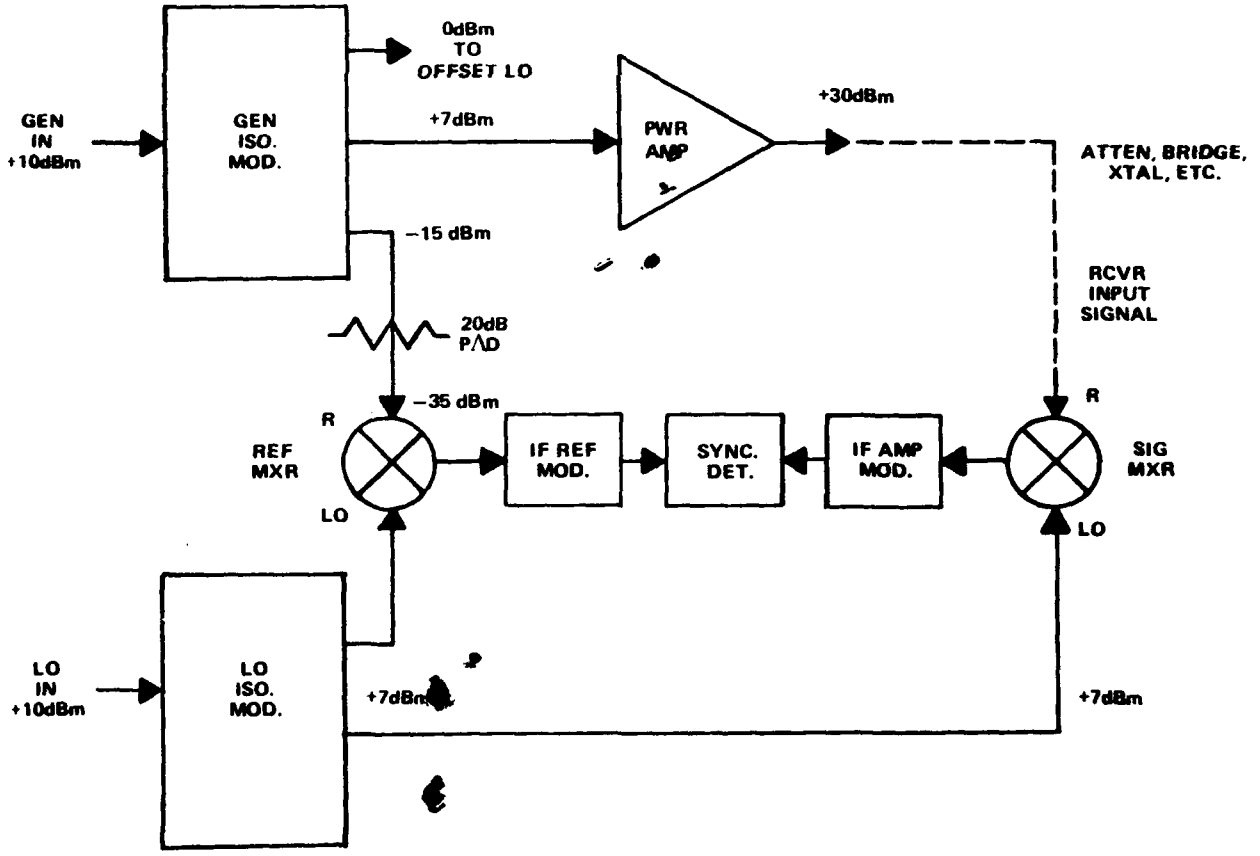


FIGURE 4.8.1.1. BASIC RECEIVER BLOCK DIAGRAM

The two critical isolation paths are shown in Figures 4.8.1.2 and 4.8.1.3.

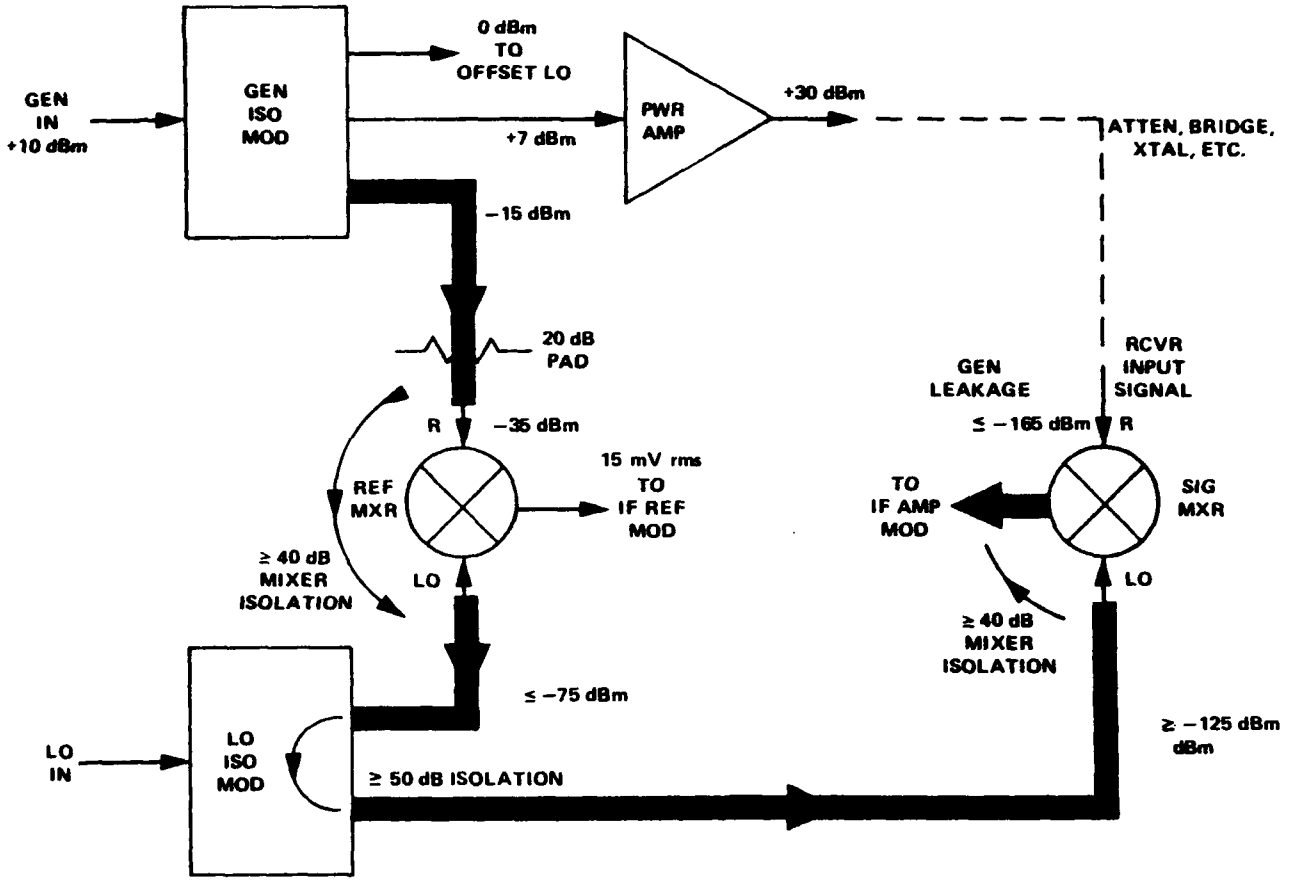


FIGURE 4.8.1.2. GENERATOR LEAKAGE PATH DIAGRAM

Spurious generator signal appears at the receiver input via a leakage path through the Reference Mixer, the LO Isolation module and the signal mixer. If each mixer has 40 dB isolation and the LO isolation module has a 50 dB isolation, the total isolation is 130 dB. An additional 20 dB is obtained by a pad at the Ref. Mixer signal Port. Starting at a level of -15 dBm from the Generator Isolation Module, the maximum leakage level is -165 dBm at the receiver input. This is below the noise level.

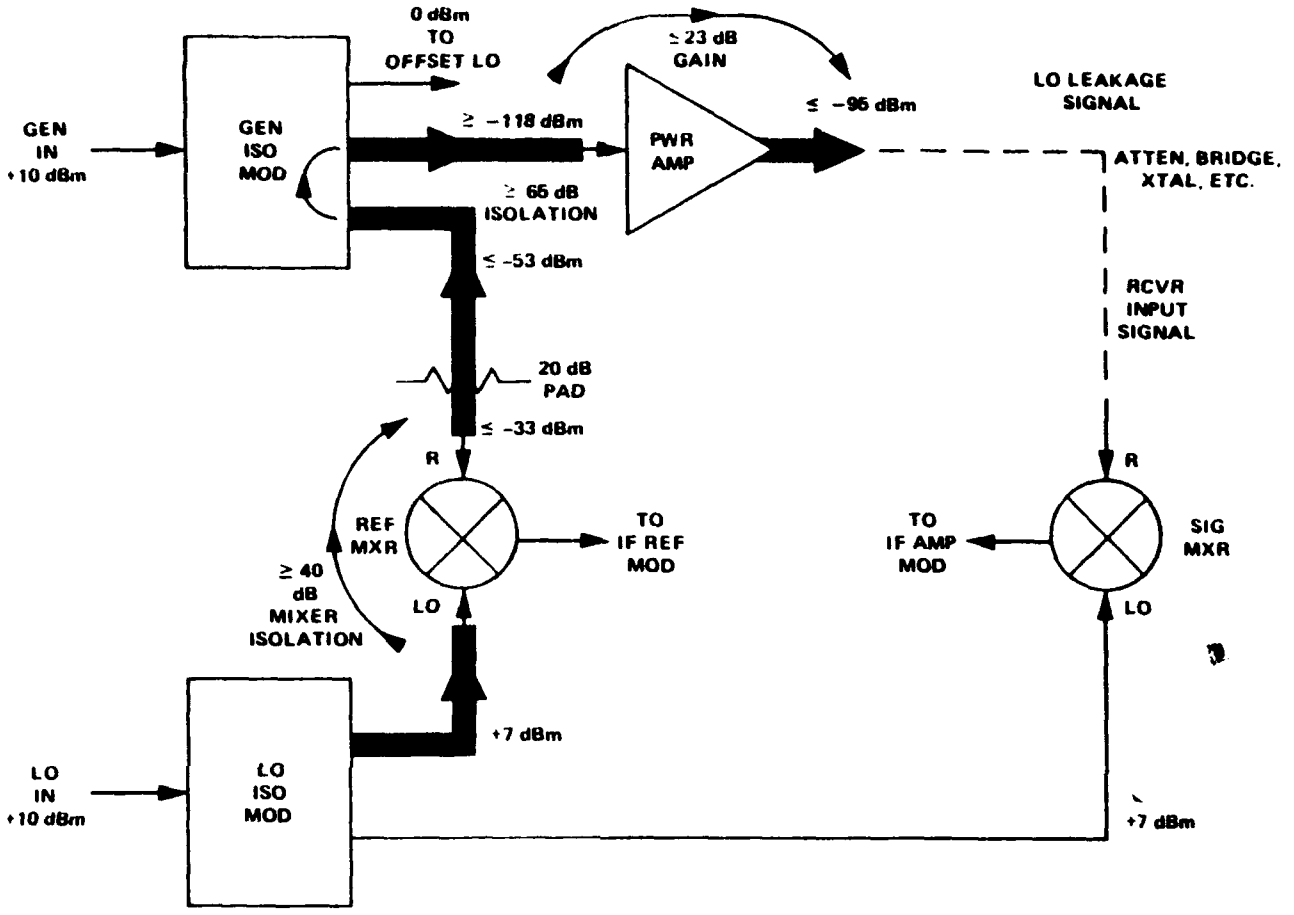


FIGURE 4.8.1.3. LOCAL OSCILLATOR LEAKAGE PATH DIAGRAM

Spurious local oscillator signal appears at the power amplifier input via a leakage path through the Reference Mixer and Generator Isolation Module. If the mixer has 40 db isolation and the Generator Isolation Module has 65 dB (from Reference Mixer to Power Amplifier ports), the total isolation is 105 dB. The additional 20 dB pad brings the total to 125 dB. Starting at a level of +7 dBm from the LO Isolation module this would result in a maximum level of -95 dBm of LO signal in the output of the power amplifier. This is easily within the -80 dBm level allowed.

The actual leakage levels obtained are greater than those calculated above because of non-ideal interface terminations but are nevertheless sufficient

to make the leakage signal undetectable below 150 MHz and within the allowed limit at all frequencies. The leakage level obtained represents about 180 dB of isolation between the power amplifier output and the receiver input.

4.8.2 Isolation Amplifier Circuits

The isolation module circuits are shown in Figures 4.8.2.1 and 4.8.2.2 The two units are quite similar. Each contains a 3 dB 180^{o} hybrid which splits the input signal into two paths with at least 20 dB isolation. One hybrid output is used directly as an output in each module. "3 dB 180^{o} Hybrid" is a Hybrid Power Splitter-Container .1 - 400 MHz mfg. by Mini-Circuit Lab #PSC-2-1, Gr #2994-5169. This reactive hybrid produces two in-phase signals isolated from each other by a minimum of 20 dB from .4 to 400 MHz with each output 3 to 4 dB less than the driving signal. The other hybrid output drives an attenuator and cascode RF amplifier to produce a highly isolated output which goes to the Reference Mixer. The generator Isolation Module contains an additional resistive power splitter which provides an output for the external Offset LO unit.

Cascode RF amplifiers were used in this application because of their high isolation and wide bandwidth. Their circuit design is straightforward. The generator unit uses A-485 transistors operating at 14 mA to produce -15 dBm output with a 50 ohm source impedance. The amplifier configuration by itself was measured to have better than 50 dB isolation to 220 MHz with a gain of +0.5 over the 0.8 to 220 MHz range.

The LO isolation module uses 2N5109 transistors operating at 33 mA to produce +12 dBm. This amplifier alone has better than 25 dB isolation to 220 MHz, a gain of 14 dB $\pm$ 1 dB over the band. An output attenuator provides a 50 ohm output impedance and reduces the output to +7 dBm.

4.8.3 Test & Performance Data

Measurements were made on the complete Generator and LO Isolation Amplifier circuit boards. The various outputs are essentially flat vs frequency

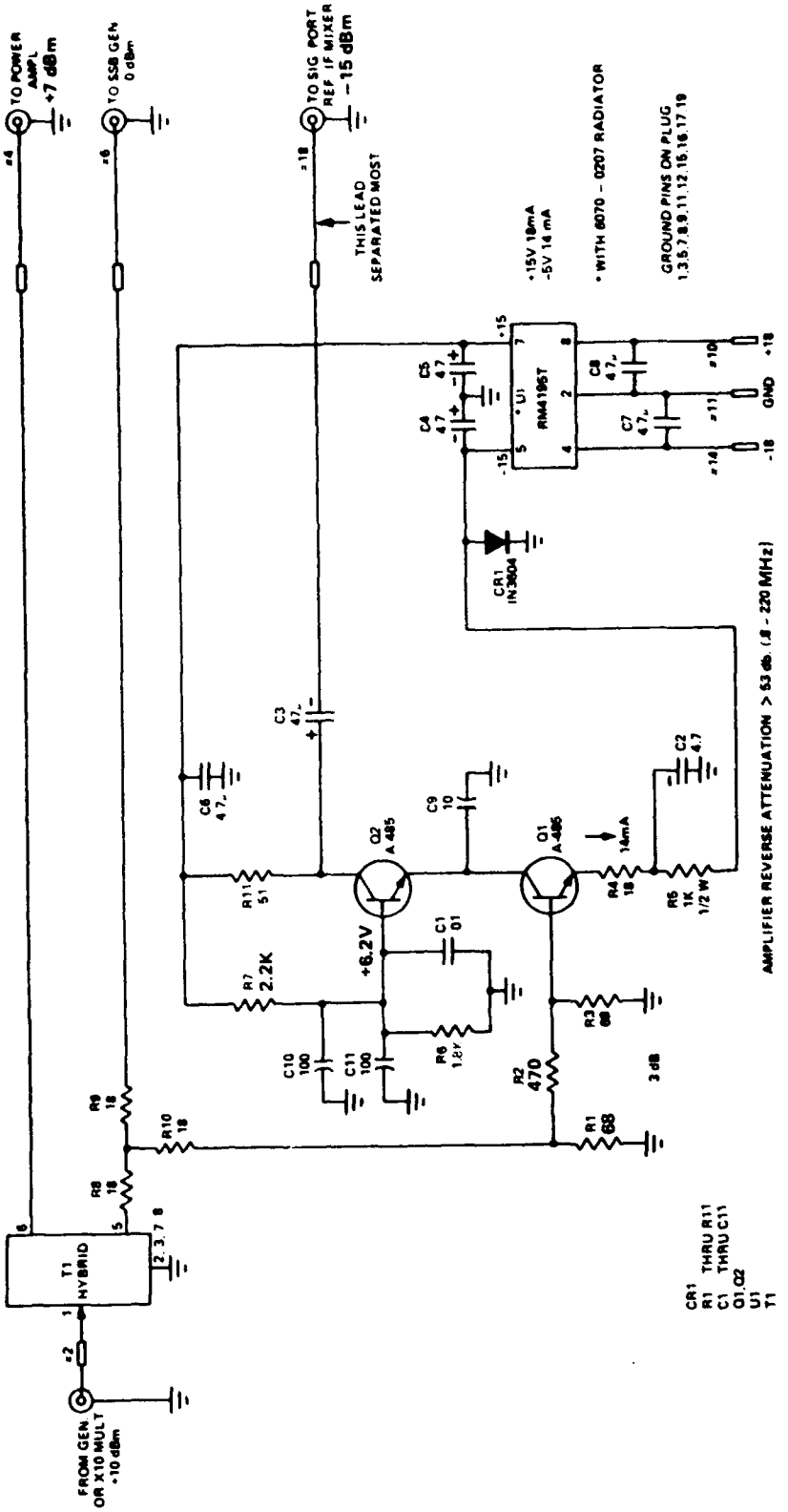


FIGURE 4.8.2.1. GENERATOR ISOLATION MODULE, SCHEMATIC DIAGRAM

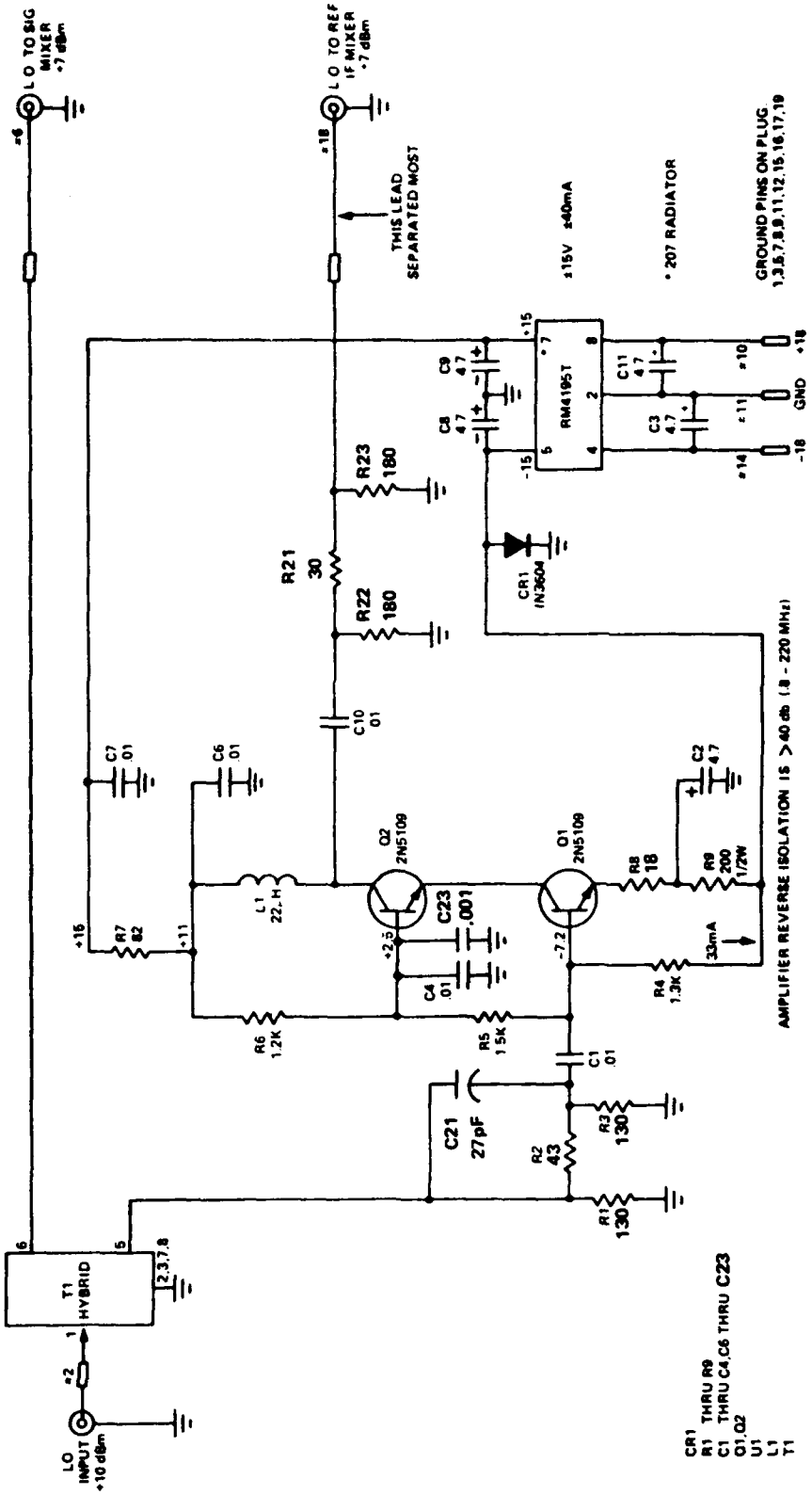


FIGURE 4.8.2.2 LOCAL OSCILLATOR ISOLATION MODULE, SCHEMATIC DIAGRAM

at the nominal level while the reverse isolation is lowest at 220 MHz. The forward and reverse characteristics of the two modules are summarized in the signal flow diagrams, Figures 4.8.3.1 and 4.8.3.2.

The isolation module performances are entirely satisfactory for the requirements of this instrument.

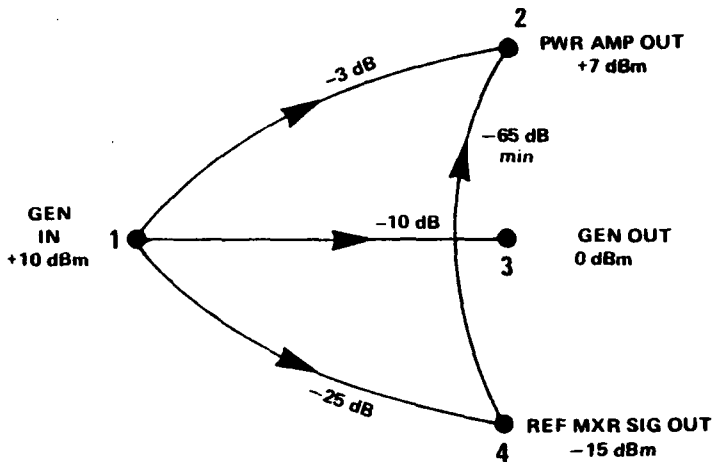


FIGURE 4.8.3.1. GENERATOR ISOLATION MODULE, SIGNAL FLOW DIAGRAM

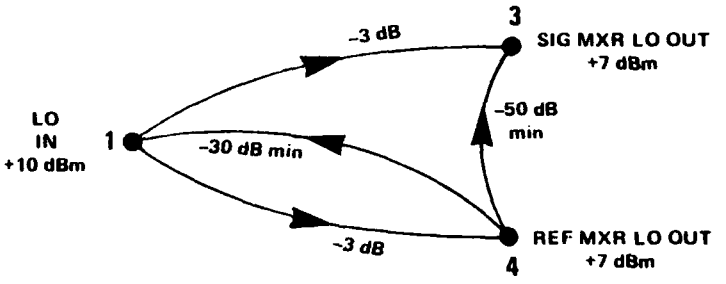


FIGURE 4.8.3.2. LOCAL OSCILLATOR MODULE, SIGNAL FLOW DIAGRAM

4.9 Mechanical Design

4.9.1 General

The Servobridge Detector is housed in a standard relay rack/bench cabinet 7" high x 16" deep. The front panel contains all operating controls along with RF connectors for generator input, RF drive to bridge, and receiver input. The Offset LO required for the receiver is not included in this unit but its operating controls are. The Offset LO is housed in a separate cabinet which can be placed under the Servobridge Detector cabinet and all interconnections are made at the rear.

All critical modules are enclosed in separate shielded compartments. The individual compartments are interconnected by means of semirigid .085 inch diameter coax for RF and flexible coax for low frequency signals. Power supply leads are run through feed-thru capacitors. Low leakage from the compartments is ensured by finger-stock contact strips.

The power supplies and the servo module are located on open boards. The servo/sweep module board also contains the RF power meter circuitry.

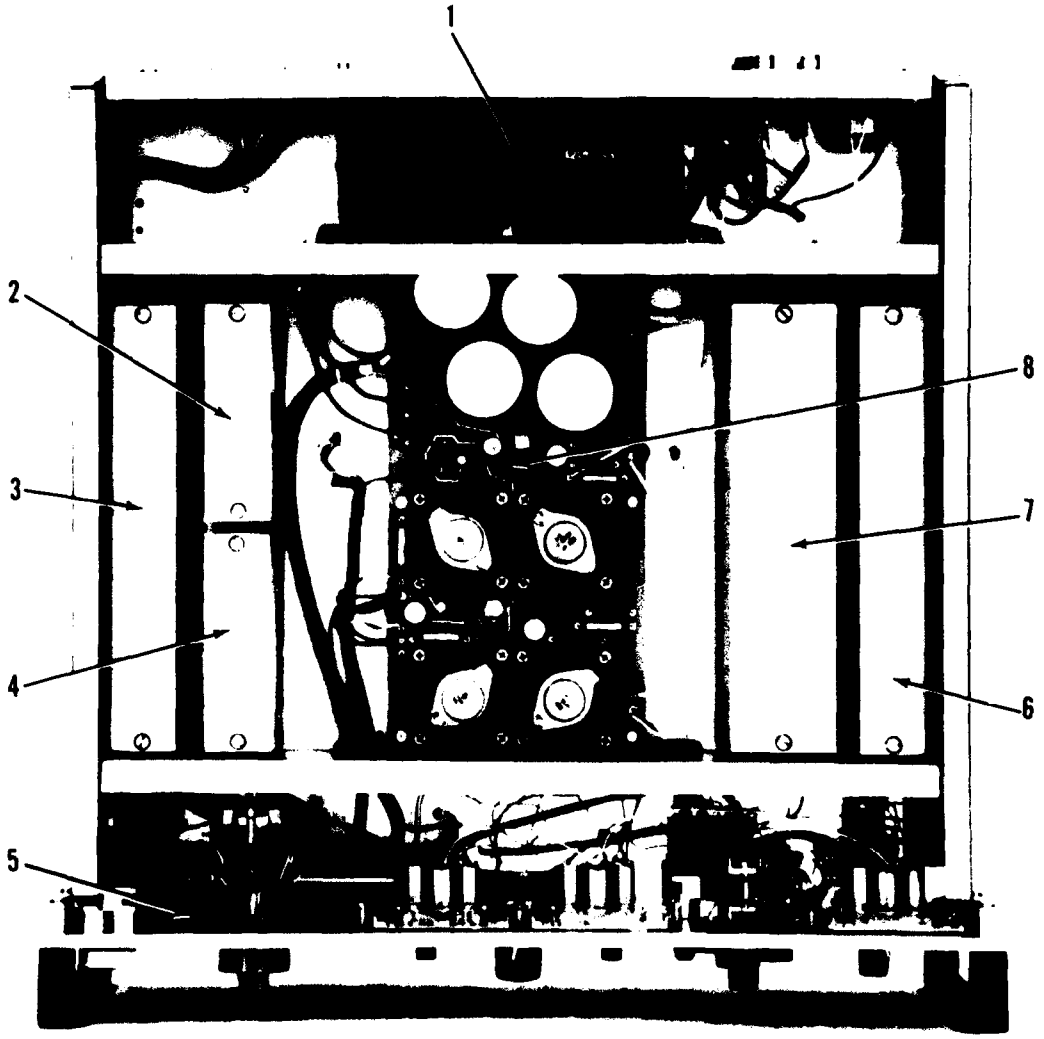
The RF power amplifier is enclosed in a casting, completely sealed against RF leakage by conductive gaskets in grooves. To dissipate the power in the RF amplifier, the unit is bolted to the aluminum front panel which acts as a good heat sink.

The modules (compartments) are as follows:

RF power amplifier

X10 multiplier

Generator isolation module



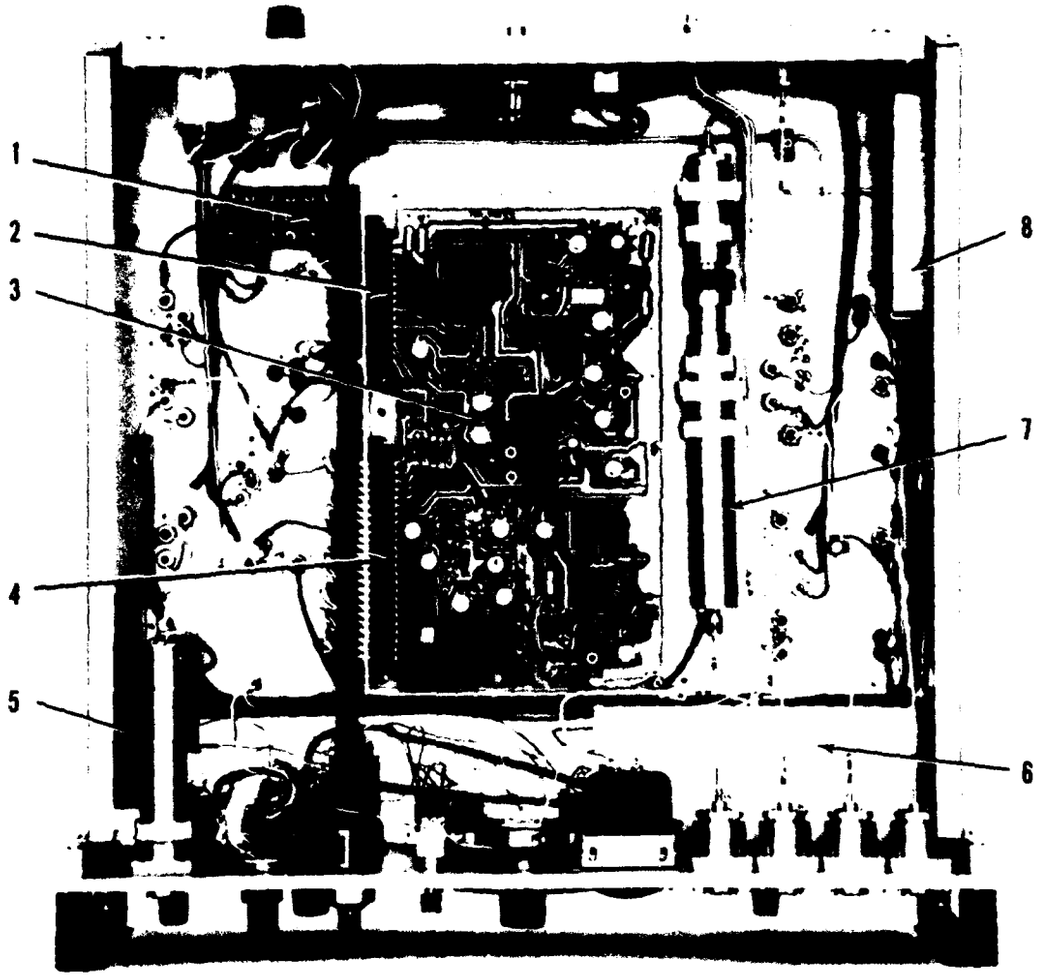
1 Power transformers, A-T1, A-T2
2 LO Isolation Module, A1
3 Frequency Multiplier Module, A2
4 Generator Isolation Module, A3
5 Step Attenuator, A4
6 IF Amplifier Module, A5
7 IF Reference and Synchronuous Detector Module, A6
8 Power Supply Etched-Circuit Board, A7

FIGURE 4.9.1.1. INTERNAL TOP VIEW OF TRACKING SERVOBRIDGE DETECTOR

LO isolation module

IF amplifier

Synchronous detectors and reference phase-shifter



1	Terminal Block, TB1	5	Receiver Mixer, A9
2	Edge Connector, A-P2	6	RF Power Amplifier Module, A10
3	Servo/Sweep Module, A8	7	Reference Mixer, A11
4	Edge Connector, A-P1	8	Tool Kit.

FIGURE 4.9.1.2. INTERNAL BOTTOM VIEW OF TRACKING SERVOBRIDGE DETECTOR

Two additional, open boards contain the power supplies and the servo/sweep circuitry.

These are shown in the top and bottom views of Figure 4.9.1.1 and 4.9.1.2.

The mechanical design was dictated, primarily, by the extremely critical shielding requirements. The power amplifier produces +30 dBm and the receiver has a detectivity of better than -150 dBm. The shielding required to prevent leakage signals through this direct path is therefore 180 dB. This high degree of shielding was attained with the mechanical arrangement as described above.

4.9.2 Panel Layouts

The layout of the front panel is shown in Figure 4.9.2.1. Table 4.9.2.1 lists the controls, indicators and connectors on the front panel and provides a brief functional description of each item.

The layout of the rear panel is shown in Figure 4.9.2.2. Table 4.9.2.2 lists the controls and connectors on the rear panel and provides a brief functional description of each item.

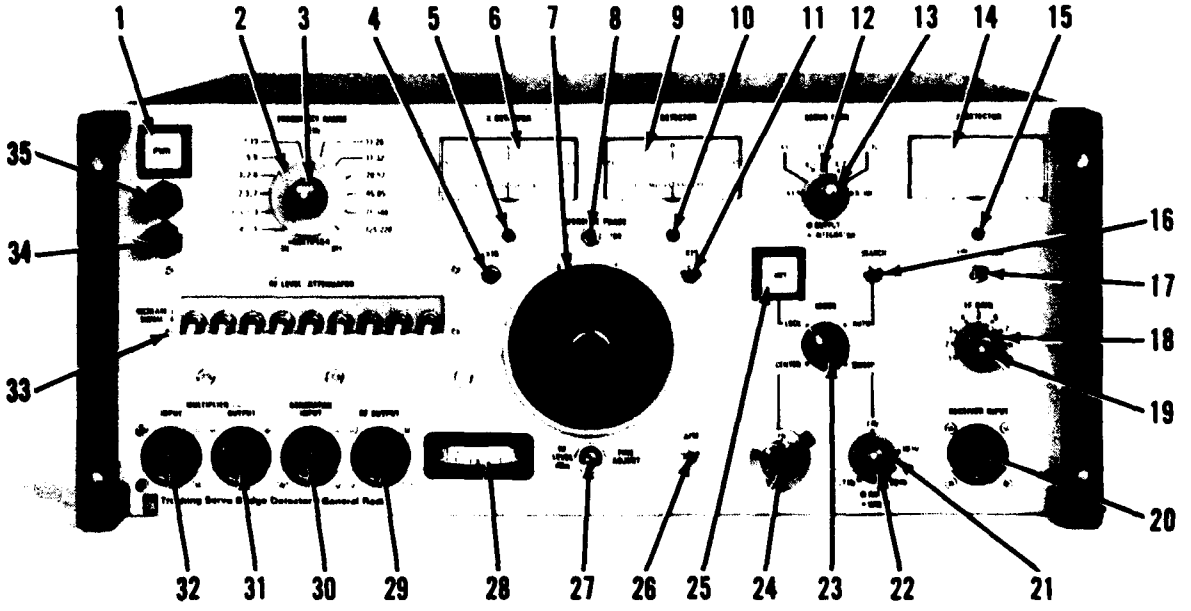


FIGURE 4.9.2.1. FRONT PANEL CONTROLS, INDICATORS, AND CONNECTORS

Table 4.9.2.1. Function of Front Panel Controls, Indicators and Connectors

Index No.	Legend	Description	Function
1	PWR	White illuminated, alternate-action pushbutton switch AS1	Turns AC line power on or off
2	FREQUENCY RANGE	14-position rotary switch A-S3A	Selects frequency range
3	MULTIPLIER ON-OFF	2-position rotary switch A-S3B	Turns frequency multiplier on or off
4	X10	Momentary contact pushbutton switch A-S4	Multiplies X Detector meter sensitivity by 10
5	none	Screwdriver control	Adjusts mechanical zero of X DETECTOR meter
6	X DETECTOR	panel meter A-M1	Indicates X Detector output
7	REFERENCE PHASE	control A-R1	Shifts detector reference phase over 360° range
8	REFERENCE PHASE 0 - 180°	Toggle switch A-S14	Shifts detector reference phase by 180°
9	Y DETECTOR	panel meter A-M2	Indicates Y Detector output
10	none	Screwdriver control	Adjusts mechanical zero of Y DETECTOR meter
11	X10	Momentary contact pushbutton switch A-S5	Multiplies Y Detector meter sensitivity by 10
12	SERVO GAIN OUTPUT	4-position rotary switch A-S7	Adjusts servo gain at control output
13	SERVO GAIN INTEGRATOR	3-position rotary switch A-S6	Adjusts servo gain at integrator
14	A DETECTOR	panel meter A-M3	Indicates IF amplifier output level.

Table 4.9.2.1. Function of Front Panel Controls, Indicators and Connectors (Cont.)

Index No.	Legend	Description	Function
15	none	Screwdriver control	Adjusts mechanical zero of A DETECTOR meter
16	SEARCH	Momentary contact push-button switch A-58	Initiates automatic search and lock cycle
17	LIN-LOG	Toggle switch A-S12	Selects linear or logarithmic IF amplifier response
18	IF GAIN	Outer knob - 9-position rotary switch A-S10	Coarse adjustment of linear mode IF gain in approx. 13 dB steps
19	IF GAIN	Center knob of dual concentric control A-R4	Provides fine adjustment of linear mode IF gain over approx. 13 dB range
20	RECEIVER INPUT	Locking type GR 874 coaxial connector A-J7	Accepts Receiver input signal
21	SWEEP RATE	Outer knob of dual concentric control A-R2A	Adjusts sweep rate over 0.1 to 50 Hz range
22	SWEEP WIDTH	Center knob of dual concentric control A-R2B	Adjusts sweep width
23	MODE	4-position rotary switch A-S9	Selects servo/sweep mode
24	CENTER	10-turn potentiometer A-R3	Adjusts control output center voltage
25	INT	Green illuminated, alternate-action push-button switch A-S11	Turns servo integrator on or off
26	Δ FM	Momentary contact push-button switch A-S13	Activates ΔFM sweep mode and display
27	RF LEVEL dBm FINE ADJUST	Screwdriver adjusted control A-R90	Sets RF output over 1 dB range

Table 4.9.2.1. Function of Front Panel Controls, Indicators and Connectors (Cont.)

Index No.	Legend	Description	Function
28	none	panel meter, A-M4	Indicates RF output power level ahead of attenuator. Also indicates low or high generator input level.
29	RF OUTPUT	Locking type GR 874 coaxial connector, A-J5	Provides RF output signal
30	GENERATOR INPUT	Locking type GR 874 coaxial connector, A-J4	Receives generator input signal (+10 dBm nominal)
31	MULTIPLIER OUTPUT	Locking type GR 874 coaxial connector, A-J3	Provides frequency multiplier output signal (+10 dBm nominal)
32	MULTIPLIER INPUT	Locking type GR 874 coaxial connector, A-J2	Receives frequency multiplier input signal (+10 dBm nominal)
33	RF LEVEL ATTENUATOR	0 to 101 dB step attenuator, A4	Sets RF output power
34	LO	Red indicator, A-DS1	Indicates unlocked local oscillator
35	MULT	Red indicator, A-DS2	Indicates unlocked frequency multiplier

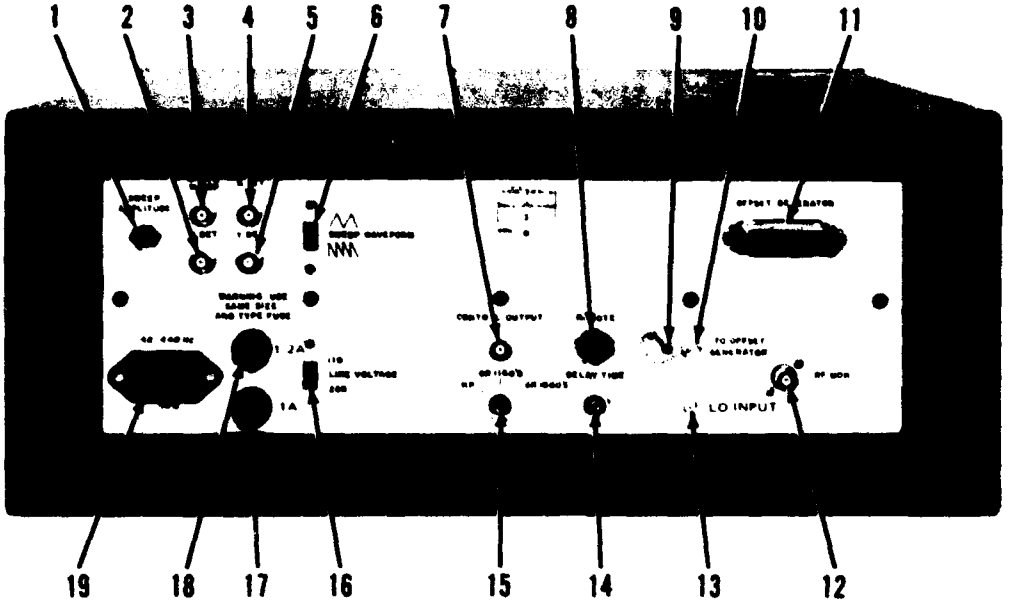


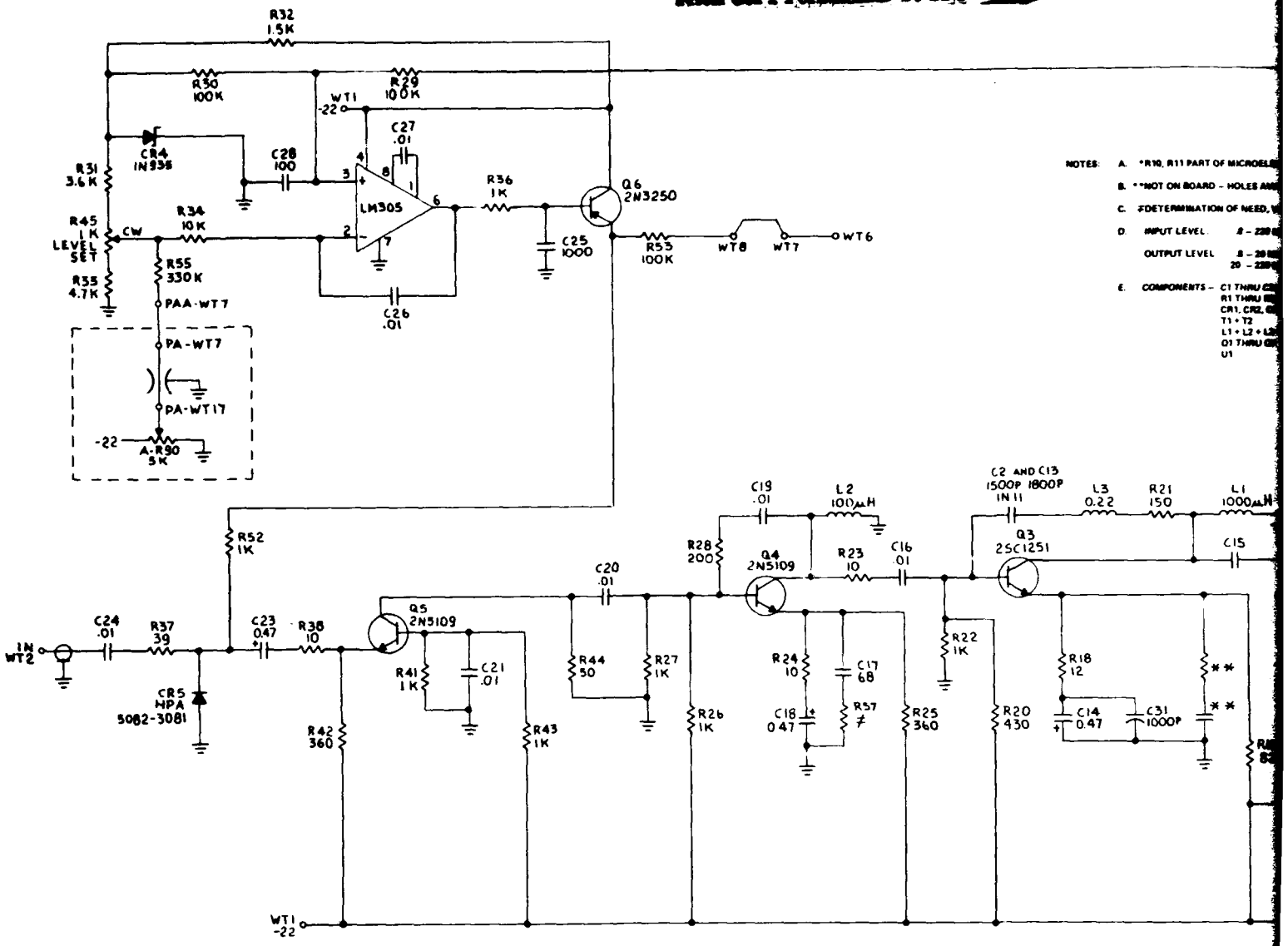
FIGURE 4.9.2.2. REAR PANEL ADJUSTMENTS AND CONNECTORS

Table 4.9.2.2. Function of Rear Panel Adjustment and Connectors

Index No.	Legend	Description	Function
1	SWEEP AMPLITUDE	Screwdriver control, A-R22	Adjusts oscilloscope horizontal sweep amplitude
2	X DET	BNC coaxial connector, A-J28	Provides X Detector output signal
3	SCOPE SWEEP	BNC coaxial connector, A-J29	Provides horizontal sweep signal to oscilloscope
4	A DET	BNC coaxial connector, A-J27	Provides A Detector output signal
5	Y DET	BNC coaxial connector, A-J26	Provides Y Detector output signal
6	SWEEP WAVEFORM	2-position slide switch, A-S20	Selects triangular or sawtooth sweep waveform
7	CONTROL OUTPUT	BNC coaxial connector, A-J25	Provides frequency control signal to synthesizer

Table 4.9.2.2. Function of Rear Panel Adjustment and Connectors (Cont.)

Index No.	Legend	Description	Function
8	REMOTE	7-pin connector (mates with Amphenol 126-195) A-J24	Provides signal for interface remote operation
9	none	50-ohm termination (on chain) A-P23	Terminates generator output when signal is not used
10	TO OFFSET GENERATOR	SMA coaxial connector A-J23	Provides generator signal to Offset local oscillator
11	OFFSET GENERATOR	24-pin connector (mates with Amphenol 57-30240) A-J30	Provides power, range, and monitor signals to Offset Local Osicillator accessory
12	RF MON	BNC coaxial connector A-J31	Provides RF frequency monitor output
13	LO IN	SMA coaxial connector A-J22	Receives local oscillator input signal
14	DELAY TIME	Screwdriver control A-R20	Adjusts delay time interval
15	HP GR 1160's GR 1060's	3-position rotary switch A-S21	Selects type of external synthesizer
16	LINE VOLTAGE	2-position slide switch A-S2	Selects line voltage
17	1A	Fuse A-F2	Protects instrument when connected to 220VAC source
18	1/2A	Fuse A-F1	Protects instrument when connected to 110VAC source
19	48 - 440 Hz 50W	3-wire IEC standard line voltage plug A-J1	Provides for primary power input



NOTES:
A. *R10, R11 PART OF MICROEL
B. **NOT ON BOARD – HOLES AV
C. ≠DETERMINATION OF NEED,
D. INPUT LEVEL .8 – 2.2
OUTPUT LEVEL .8 – 20
20 – 22
E. COMPONENTS – C1 THRU C
R1 THRU
CR1, CR2,
T1 + T2
L1 + L2 + L
Q1 THRU
U1

BOARD

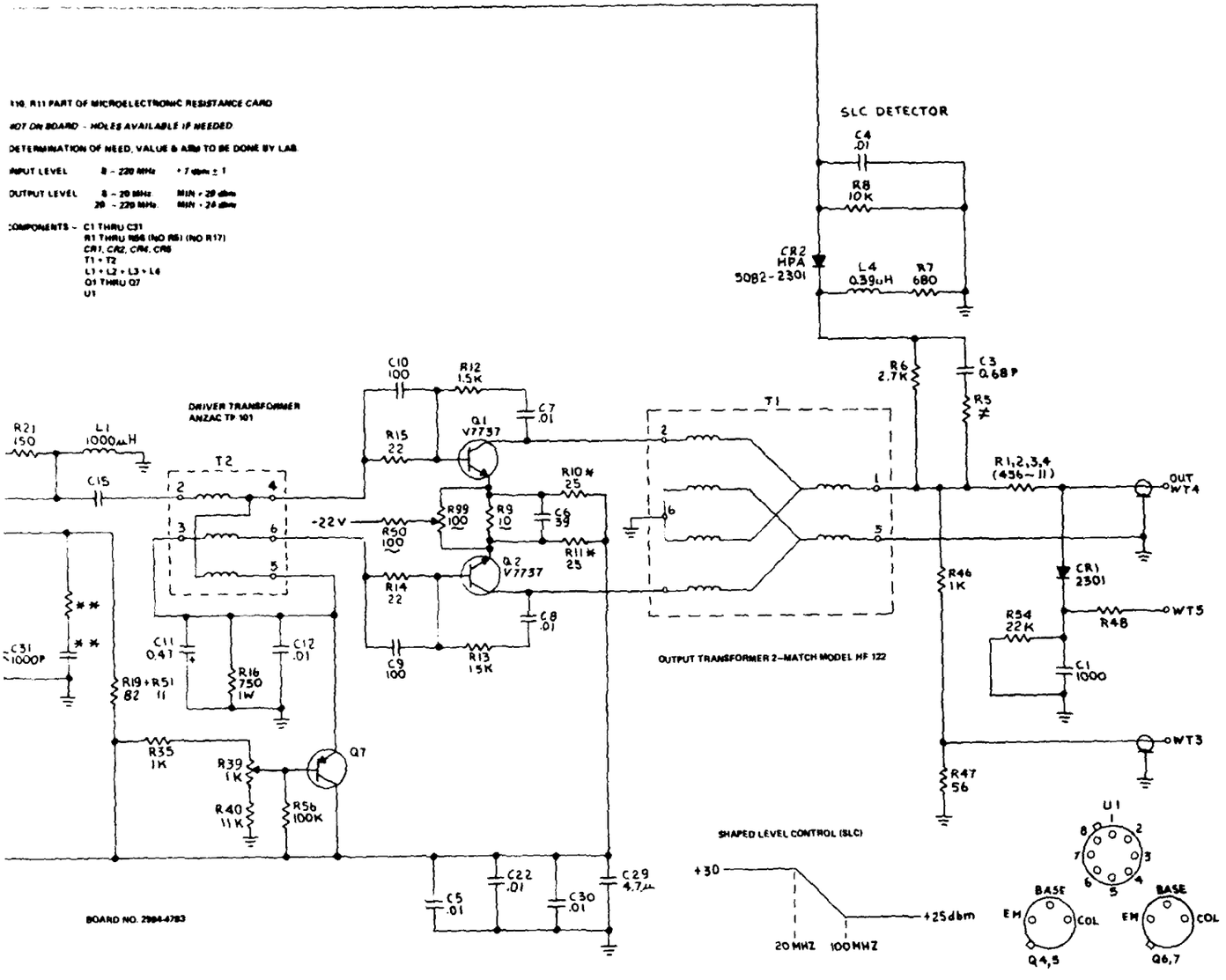


Figure 4.10.1 RF Power Amplifier PAA MK1

2

GAIN SWITCH POSITION	NOMINAL STAGE GAIN, dB			VAR. GAIN, dB	
	1ST	2ND	3RD	MIN	MAX
1 (MIN)	VAR	0	0	0	13
2	"	"	"	13	27
3	"	"	"	27	40
4	40	VAR	"	0	13
5	"	"	"	13	27
6	"	"	"	27	40
7	"	40	VAR	0	13
8	"	"	"	13	27
9 (MAX)	"	"	"	27	40
LOG	ALL GAIN CONTROL LINES AT -15V				

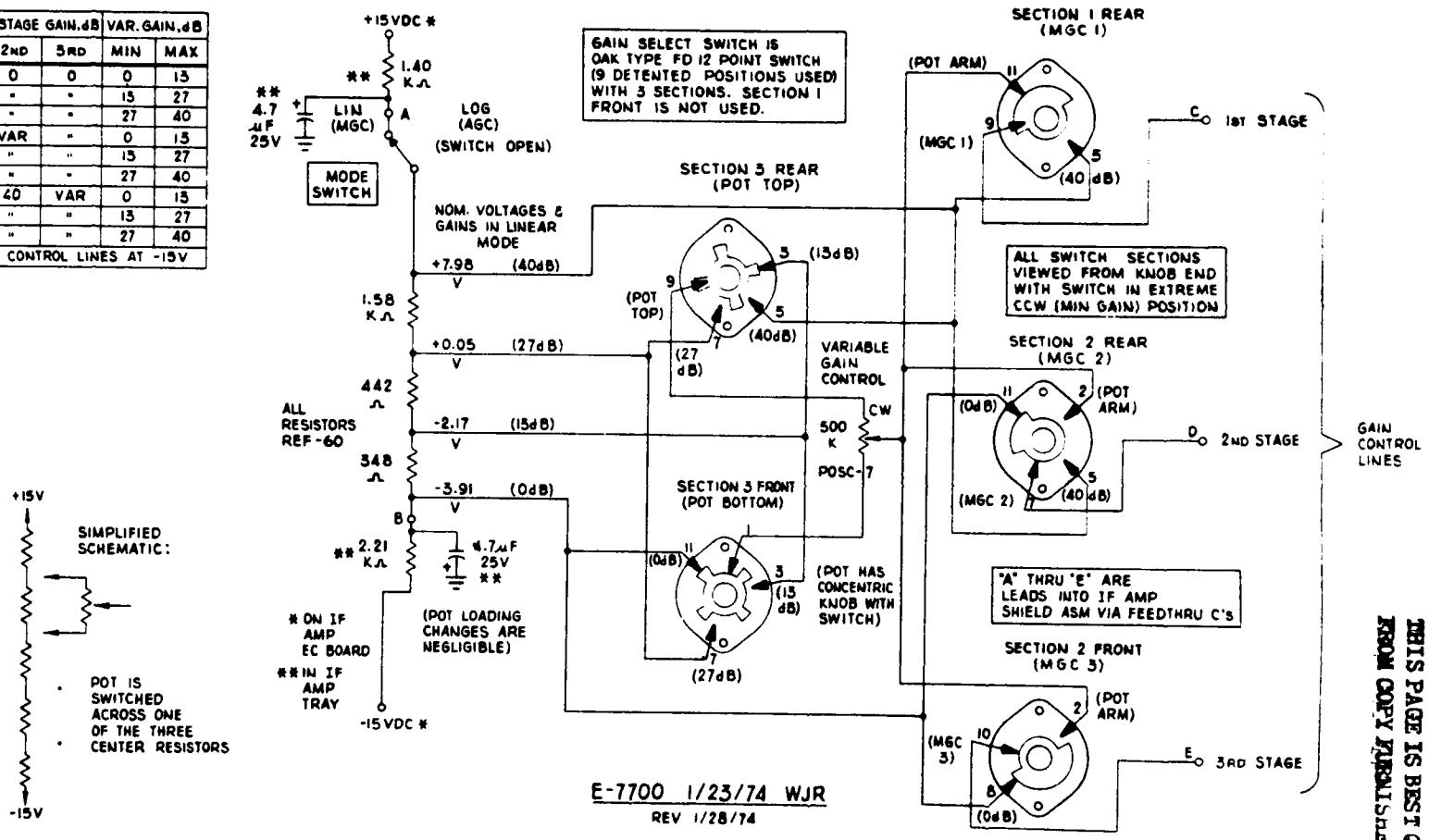


Figure 4.10.2. Mode/Gain Control Circuit For 80 kHz IF Amplifier

4.11 Wire Run List

MASTER REFERENCE DESIGNATION INDEX

REF. DESIG.	FIGURE NO.	INDEX NO.
A-1	4,9,1,1	2
A-2	4,9,1,1	3
A-3	4,9,1,1	4
A-4	4,9,1,1	5
A-5	4,9,1,1	6
A-6	4,9,1,1	7
A-7	4,9,1,1	8
A-8	4,9,1,2	3
A-9	4,9,1,2	5
A-10	4,9,1,2	6
A-11	4,9,1,2	7
A-DS1	4,9,2,1	34
A-DS2	4,9,2,1	35
A-F1	4,9,2,2	18
A-F2	4,9,2,2	16
A-J1	4,9,2,2	19
A-J2	4,9,2,1	32
A-J3	4,9,2,1	31
A-J4	4,9,2,1	30
A-J5	4,9,2,1	29
A-J7	4,9,2,1	20
A-J22	4,9,2,2	13
A-J23	4,9,2,2	10
A-J24	4,9,2,2	8
A-J25	4,9,2,2	7
A-J26	4,9,2,2	5
A-J27	4,9,2,2	4
A-J28	4,9,2,2	2
A-J29	4,9,2,2	3
A-J30	4,9,2,2	11
A-J31	4,9,2,2	12
A-M1	4,9,2,1	6
A-M2	4,9,2,1	9
A-M3	4,9,2,1	14
A-M4	4,9,2,1	28
A-P1	4,9,1,2	4
A-P2	4,9,1,2	2
A-P23	4,9,2,2	9
A-R1	4,9,2,1	7
A-R2A	4,9,2,1	21
A-R2B	4,9,2,1	22
A-R3	4,9,2,1	24
A-R4	4,9,2,1	19
A-R20	4,9,2,2	14
A-R22	4,9,2,2	1
A-R90	4,9,2,1	27
A-S1	4,9,2,1	1
A-S3A	4,9,2,1	2
A-S3B	4,9,2,1	3
A-S4	4,9,2,1	4
A-S5	4,9,2,1	11
A-S6	4,9,2,1	13
A-S7	4,9,2,1	12
A-S8	4,9,2,1	16
A-S9	4,9,2,1	23
A-S10	4,9,2,1	18
A-S11	4,9,2,1	25
A-S12	4,9,2,1	17
A-S13	4,9,2,1	26
A-S14	4,9,2,1	8
A-S20	4,9,2,2	6
A-S21	4,9,2,2	15
A-T1	4,9,1,1	1
A-T2	4,9,1,1	1
TB1	4,9,1,2	1

WIRE LIST ABBREVIATIONS

Adj.	Adjacent	GND	Ground
AWG	American Wire Gauge	GY	Gray
BK	Black	OR	Orange
BR	Brown	RD	Red
BU	Blue	VT	Violet
COND	Conductor (center)	WH	White
GN	Green	YE	Yellow

WIRE RUN LIST

FROM	WIRE TYPE	COLOR CODE	TO
A-J24-A	AWG24	WH-OR-GN	A-P1-M
A-J24-B	AWG24	WH-OR-RD	A-P1-N
A-J24-COM	AWG24	WH-BR-BK	A-P1-9
A-J24-D	AWG24	WH-OR-BK	A-P1-J
A-J24-E	AWG24	WH-VT-GN-BR	A-P1-3
A-J24-F	AWG24	WH-VT-GN-BU	A-P1-7
COND TO A-J25	COAX CABLE	BR-YE	COND TO A-P2-1
SHIELD TO ADJ. GND			SHIELD TO A-P2-A
A-J27 CENTER	AWG24	WH-RD-GN-BK	A-P2-8
A-J30-1	AWG24	WH-BU-BK	A-S3A-103F
A-J30-2	AWG24	WH-BU-BR	A-S3A-105F
A-J30-3	AWG24	WH-GR-BK	A-S3A-107F
A-J30-4	AWG24	WH-GR-BR	A-S3A-109F
A-J30-5	AWG24	WH-GN-BU	A-S3A-111F
A-J30-6	AWG24	WH-RD-BK	A-S3A-113F
A-J30-7	AWG24	WH-RD-BR	A-S3A-115F
A-J30-8	AWG24	WH-RD-BU	A-S3A-117F
A-J30-9	AWG24	WH-RD-GN	A-S3A-119F
A-J30-10	AWG24	WH-GY-BK	A-S3A-121F
A-J30-11	AWG24	WH-GY-BR	A-S3A-123F
A-J30-12	AWG24	WH-GY-BU	A-S3A-125F
A-J30-13	AWG20	GN	A7-WT5
A-J30-14	AWG20	WH-BK	GROUND
A-J30-16	AWG20	BR	A7-WT7
A-J30-17	AWG20	WH-BK	GROUND
A-J30-19	AWG20	RD	A7-WT14
A-J30-20	AWG20	WH-BK	GROUND
A-J30-22	AWG20	OR	A7-WT12
A-J30-23	AWG20	WH-BK	GROUND
A-J30-24	AWG24	WH-VT-BK	A-XDS1-2
A-M3(-)	AWG24	WH-BK	GROUND
A-M4(+)	AWG24	WH-GN-BU	A-P1-5
A-P1-A	AWG24	WH-VT-BK	A-R2A-3
A-P1-AA	AWG24	WH-YE-VT	A-S21-203R
A-P1-B	AWG24	WH-VT-BR	A-S20-4
A-P1-BB	AWG24	WH-YE-OR	A-S21-205R
A-P1-C	AWG24	WH-VT-BU	A-S20-6
A-P1-D	AWG24	WH-VT-GN	A-R2B-3
A-P1-E	AWG24	WH-BU-BR-BK	A-P2-14
A-P1-E	AWG24	WH-BU-BR-BK	A-S9-204F
A-P1-F	AWG24	WH-VT-RD	A-R20-COM
A-P1-H	AWG24	WH-VT-GY	A-R20-COM
A-P1-J	AWG24	WH-OR-BK	A-J24-D
A-P1-K	AWG24	WH-OR-BR	A-S9-301F
A-P1-L	AWG24	WH-OR-BU	A-S9-201F
A-P1-M	AWG24	WH-OR-GN	A-J24-A
A-P1-N	AWG24	WH-OR-RD	A-J24-B

WIRE RUN LIST (CONT)

FROM	WIRE TYPE	COLOR CODE	TO
A-P1-P	AGW24	WH-OR-GY	A-S21-105R
A-P1-R	AGW24	WH-OR-VT	A7-WT15
A-P1-U	AGW24	WH-YE-BK	A7-WT16
A-P1-V	AGW24	WH-YE-BR	A-S9-208R
A-P1-W	AGW24	WH-YE-BU	A-S7-105R
A-P1-X	AGW24	WH-YE-GN	A-S7-103R
A-P1-Y	AGW24	WH-YE-RD	A-S7-101R
A-P1-Z	AGW24	WH-YE-GY	A-S21-207R
A-P1-1	AGW24	WH-BR	A-R2A-2
A-P1-10	AGW24	WH-BU-BK	A-S11-3(C)
A-P1-11	AGW24	WH-BU-BR	A-R1-2
A-P1-12	AGW24	WH-GN-BK	A6-36
A-P1-13	AGW24	OR	A-S9-106R
A-P1-13	AGW24	OR	A-P2-6
A-P1-14	AGW24	WH-GN-BR	A-S21-103R
A-P1-16	AGW24	WH-RD-BK	A-S21-101R
A-P1-17	AGW24	WH-RD-BR	A-S9-304F
A-P1-18	AGW24	WH-RD-BU	A-S9-203F
A-P1-19	AGW24	WH-RD-GN	A-S7-107R
A-P1-2	AGW24	WH-BU	A-S20-5
A-P1-20	AGW24	WH-GY-BK	A-S21-102R
A-P1-21	AGW24	WH-GY-BR	A-S21-211R
A-P1-22	AGW24	WH-GY-BU	A-S21-209R
A-P1-23	AGW24	WH-GY-GN	A-S21-201R
A-P1-24	AGW24	WH-GY-RD	A-S21-208R
A-P1-3	AGW24	WH-VT-GN-BU	A-J24-E
A-P1-3	AGW24	WH-GN	A-S8-N.O.
A-P1-4	AGW24	WH-RD	A-S9-103F
A-P1-5	AGW24	WH-GN-BU	A-M4-(+)
A-P1-5	AGW24	WH-GY	A-R2B-2
A-P1-6	AGW24	WH-VT	A-S13-N.O.
A-P1-7	AGW24	WH-VT-GN-BU	A-J24-F
A-P1-7	AGW24	WH-OR	A-S8-CENTER
A-P1-8	AGW24	WH-YE	A-R22-(CCW)
A-P1-9	AGW24	WH-BR-BK	A-J24-COM
A-P2-B	AGW24	WH-GY-BU-BK	A-S21-108R
A-P2-C	AGW24	WH-GY-BU-BR	A-P2-S
A-P2-D	AGW24	WH-GY-GN-BK	A-S21-111R
A-P2-E	AGW24	WH-GY-GN-BR	A-S21-107R
A-P2-F	AGW24	OR	A-P2-15
A-P2-F	AGW24	OR	A-P2-6
A-P2-H	AGW24	WH-GY-GN-BU	A-S21-109R
COND TO A-P2-J	COAX CABLE	BR-OR	COND TO A6-22 SHIELD TO ADJ. GND
A-P2-K	AGW24	WH-VT-GY-RD	A-R604 (FREE END)
COND TO A-P2-K	COAX CABLE	BR-GN	COND TO A5-45
SHIELD TO A-P2-L			SHIELD TO GROUND
A-P2-M	AGW24	WH-GY-BU-BK	A-S11-1(N.C.)

WIRE RUN LIST (CONT)

FROM	WIRE TYPE	COLOR CODE	TO
A-P2-N	AWG24	WH-GY-BU-BR	A-S6-4F
A-P2-P	AWG24	WH-GY-GN-BK	A-S6-5F
A-P2-R	AWG24	WH-GY-GN-BR	TB1-18V
A-P2-S	AWG24	WH-GY-BU-BR	A-P2-C
A-P2-S	AWG24	WH-BK	GROUND
COND TO A-P2-1	COAX CABLE	BR-YE	COND TO A-J25
SHIELD TO A-P2-A			SHIELD TO ADJ. GND
A-P2-1	AWG24	WH-GN-BR-BK	A-S21-202R
COND TO A-P2-10	COAX CABLE	BR-RD	COND TO A6-33
(NO GND CONNECTION THIS END)			SHIELD TO GND
A-P2-13	AWG24	WH-GY-BR-BK	A-S6-1F
A-P2-14	AWG24	WH-BU-BR-BK	A-P1-E
A-P2-15	AWG24	OR	TB1-+18V
A-P2-15	AWG24	OR	A-P2-F
A-P2-2	AWG24	WH-GN-BU-BK	A-S7-104R
A-P2-3	AWG24	WH-GN-BU-BR	A-R3-2
A-P2-4	AWG24	WH-RD-BR-BK	A-R3-1
A-P2-5	AWG24	WH-RD-BU-BK	A-R3-3
A-P2-6	AWG24	OR	A-P2-F
A-P2-6	AWG24	OR	A-P1-13
A-P2-7	AWG24	WH-RD-BU-BR	A-S9-206R
A-P2-8	AWG24	WH-RD-GN-BK	A-J27 CENTER
A-P2-9	AWG24	WH-RD-GN-BR	A-S9-107F
A-R1-1	AWG24	WH-VT-GY-GN	PS-37
A-R1-2	AWG24	WH-VT-GY-BU	SP-36
A-R1-2	AWG24	WH-BU-BR	A-P1-11
A-R1-3	AWG24	WH-VT-GY-BR	PS-35
A-R2A-2	AWG24	WH-BR	A-P1-1
A-R2A-3	AWG24	WH-VT-BK	A-P1-A
A-R2B-1	AWG24	WH-BK	GROUND
A-R2B-2	AWG24	WH-GY	A-P1-5
A-R2B-2	AWG24	YE	A-S9-202-R
A-R2B-3	AWG24	WH-VT-GN	A-P1-D
A-R20-COM	AWG24	WH-VT-GY	A-P1-H
A-R20-COM	AWG24	WH-VT-RD	A-P1-F
A-R22 (CW)	AWG24	VT	A-S9-104F
A-R22 (CCW)	AWG24	WH-YE	A-P1-8
A-R3-1	AWG24	WH-RD-BR-BK	A-P2-4
A-R3-2	AWG24	WH-GN-BU-BR	A-P2-3
A-R3-3	AWG24	WH-RD-BU-BK	A-P2-5
A-R604 (FREE END)	AWG24	WH-VT-GY-RD	A-P2-K
A-R90-CW	AWG20	GN	A7-WT5
A-S10-109R	AWG24	WH-RD	A5-14
A-S10-207G	AWG24	WH-GY	A5-17
A-S10-210F	AWG24	WH-VT	A5-33
A-S10-305R	AWG24	WH-YE	A-S12-#5
A-S10-311F	AWG24	WH-OR	A5-31
A-S11-B (LAMP)	AWG24	WH-BK	GROUND

WIRE RUN LIST (CONT)

FROM	WIRE TYPE	COLOR CODE	TO
A-S11-1 (N.C.)	AWG24	WH-GY-BU-BK	A-P2-M
A-S11-3(C)	AWG24	WH-BU-BK	A-P1-10
A-S11-#6 (COM)	AWG24	GY	A-S9-308R
A-S12-#3	AWG24	WH-BR-BK	A5-19
A-S12-#5	AWG24	WH-YE	A-S10-305R
A-S13-CENTER	AWG24	BU	A-S9-108R
A-S13-N.O.	AWG24	WH-VT	A-P1-6
A-S14-3	AWG24	YE	A6-31
A-S20-4	AWG24	WH-VT-BR	A-P1-B
A-S20-5	AWG24	WH-BU	A-P1-2
A-S20-6	AWG24	WH-VT-BU	A-P1-C
A-S21-101R	AWG24	WH-RD-BK	A-P1-16
A-S21-102R	AWG24	WH-GY-BK	A-P1-20
A-S21-103R	AWG24	WH-GN-BR	A-P1-14
A-S21-105R	AWG24	WH-OR-GY	A-P1-P
A-S21-107R	AWG24	WH-GY-GN-BR	A-P2-E
A-S21-108R	AWG24	WH-GY-BU-BK	A-P2-B
A-S21-109R	AWG24	WH-GY-GN-BU	A-P2-H
A-S21-111R	AWG24	WH-GY-GN-BK	A-P2-D
A-S21-201R	AWG24	WH-GY-GN	A-P1-23
A-S21-202R	AWG24	WH-GN-BR-BK	A-P2-1
A-S21-203R	AWG24	WH-YE-VT	A-P1-AA
A-S21-205R	AWG24	WH-YE-OR	A-P1-BB
A-S21-207R	AWG24	WH-YE-GY	A-P1-Z
A-S21-208R	AWG24	WH-GY-RD	A-P1-24
A-S21-209R	AWG24	WH-GY-BU	A-P1-22
A-S21-211R	AWG24	WH-GY-BR	A-P1-21
A-S3A-103F	AWG24	WH-BU-BK	AJ30-1
A-S3A-104R	AWG24	WH-GY-GN	A-S3B-127R
A-S3A-104R	AWG24	GN	A7-WT5
A-S3A-105F	AWG24	WH-BU-BR	AJ30-2
A-S3A-107F	AWG24	WH-GR-BK	AJ30-3
A-S3A-109F	AWG24	WH-GR-BR	AJ30-4
A-S3A-111F	AWG24	WH-GN-BU	AJ30-5
A-S3A-113F	AWG24	WH-RD-BK	AJ30-6
A-S3A-115F	AWG24	WH-RD-BR	AJ30-7
A-S3A-117F	AWG24	WH-RD-BU	AJ30-8
A-S3A-118R	AWG24	WH-VT-BU	A-S3B-122F
A-S3A-119F	AWG24	WH-RD-GN	AJ30-9
A-S3A-121F	AWG24	WH-GY-BK	AJ30-10
A-S3A-122R	AWG24	WH-VT-GY	A2-2
A-S3A-123F	AWG24	WH-GY-BR	AJ30-11
A-S3A-124R	AWG24	WH-OR-BK	A2-20
A-S3A-125F	AWG24	WH-GY-BU	AJ30-12
A-S3A-126R	AWG24	WH-OR-BR	A2-9
A-S3B-112R	AWG24	WH-GY-RD	A-XDS1-1
A-S3B-116F	AWG24	WH-VT-BR	A-XDS2-1

WIRE RUN LIST (CONT)

FROM	WIRE TYPE	COLOR CODE	TO
A-S3B-122F	AWG24	WH-VT-BU	A-S3A-118R
A-S3B-124R	AWG24	GN	A7-WT5
A-S3B-127R	AWG24	WH-GY-GN	A-S3A-104R
S3B-128F	AWG24	WH-VT-GN	A2-32
A-S4-N.O.	AWG24	WH-GY-GN-BU	A6-33
A-S5-N.O.	AWG24	WH-GY-BR-BK	A6-22
A-S6-1F	AWG24	WH-GY-BR-BK	A-P2-13
A-56-104F	AWG24	WH-BU	A-S9-307F
A-S6-4F	AWG24	WH-GY-BU-BR	A-P2-N
A-S6-5F	AWG24	WH-GY-GN-BK	A-P2-P
A-S7-101R	AWG24	WH-YE-RD	A-P1-Y
A-S7-103R	AWG24	WH-YE-GN	A-P1-X
A-S9-104F	AWG24	VT	A-R22-(CW)
A-S7-104R	AWG24	WH-GN-BU-BK	A-P2-2
A-S7-105R	AWG24	WH-YE-BU	A-P1-W
A-S7-107R	AWG24	WH-RD-GN	A-P1-19
A-S8-CENTER	AWG24	WH-OR	A-P1-7
A-S8-N.O.	AWG24	WH-GN	A-P1-3
A-S9-103F	AWG24	WH-RD	A-P1-4
A-S9-106R	AWG24	WH-BR	A-S9-302R
A-S9-106R	AWG24	OR	A-P1-13
A-S9-107F	AWG24	WH-RD-GN-BR	A-P2-9
A-S9-108R	AWG24	BU	A-S13-CENTER
A-S9-201F	AWG24	WH-OR-BU	A-P1-L
A-S9-202R	AWG24	YE	A-R2B-2
A-S9-203F	AWG24	WH-RD-BU	A-P1-18
A-S9-204F	AWG24	WH-BU-BR-BK	A-P1-E
A-S9-206R	AWG24	WH-RD-BU-BR	A-P2-7
A-S9-208R	AWG24	WH-YE-BR	A-P1-V
A-S9-301F	AWG24	WH-OR-BR	A-P1-K
A-S9-302R	AWG24	WH-BR	A-S9-106R
A-S9-304F	AWG24	WH-RD-BR	A-P1-17
A-S9-306R	AWG20	WH-BK	GROUND
A-S9-307F	AWG24	WH-BU	A-S6-104F
A-S9-308R	AWG24	GY	A-S11-#6(COM)
A-XDS1-1	AWG24	WH-GY-RD	A-S3B-112R
A-XDS1-2	AWG24	WH-VT-BK	AJ30-24
A-XDS2-1	AWG24	WH-VT-BR	A-S3B-116F
A-XDS2-2	AWG24	WH-VT-RD	A2-44
A220	AWG24	WH-OR-BK	A-S3A-124R
A22	AWG24	WH-VT-GY	A-S3A-122R
A2-32	AWG24	WH-VT-GN	S3B-128F
A2-42	AWG24	BR	A7-WT7
A2-44	AWG24	WH-VT-RD	A-XDS2-2
A29	AWG24	WH-OR-BR	A-S3A-126R
A5-14	AWG24	WH-RD	AS10-109R
A5-17	AWG24	WH-GY	A-S10-207G

WIRE RUN LIST (CONT)

FROM	WIRE TYPE	COLOR CODE	TO
A5-19	AWG24	WH-BR-BK	A-S12-#3
A5-31	AWG24	WH-OR	A-S10-311F
A5-33	AWG24	WH-VT	A-S10-210F
COND TO A5-45	COAX CABLE	BR-GN	COND TO A-P2-K
SHIELD TO ADJ. GND			SHIELD TO A-P2-L
A6-22	AWG24	WH-GY-BR-BK	A-S5-N.O.
COND TO A6-22	COAX CABLE	BR-OR	COND TO A-P2-J
SHIELD TO ADJ GND			
A6-31	AWG24	YE	A-S14-3
A6-33	AWG24	WH-GY-GN-BU	A-S4-N.O.
COND TO A6-33	COAX CABLE	BR-RD	COND TO A-P2-10
SHIELD TO GND			(NO GND CONNECTION THIS END)
A6-36	AWG24	WH-GN-BK	A-P1-12
A7-WT12	AWG20	OR	AJ30-22
A7-WT14	AWG20	RD	AJ30-19
A7-WT15	AWG24	WH-OR-VT	A-P1-R
A7-WT16	AWG24	WH-YE-BK	A-P1-U
A7-WT5	AWG24	GN	A-S3B-124R
A7-WT5	AWG20	GN	A-R90-CW
A7-WT5	AWG20	GN	AJ30-13
A7-WT5	AWG24	GN	A-S3A-104R
A7-WT6	AWG20	WH-BK	GROUND
A7-YWT7	AWG20	BR	AJ30-16
A7-WT7	AWG24	BR	A2-42
A7-WT8	AWG20	WH-BK	GROUND
GROUND	AWG20	WH-BK	A7-WT6
GROUND	AWG20	WH-BK	A-S9-306R
GROUND	AWG20	WH-BK	A7-WT8
GROUND	AWG20	WH-BK	AJ30-23
GROUND	AWG20	WH-BK	AJ30-20
GROUND	AWG20	WH-BK	AJ30-17
GROUND	AWG20	WH-BK	AJ30-14
GROUND	AWG24	WH-BK	A-M3(-)
GROUND	AWG24	WH-BK	A-S11-B(LAMP)
GROUND	AWG24	WH-BK	A-R2B-1
GROUND	AWG24	WH-BK	A-P2-5
PS-35	AWG24	WH-VT-GY-BR	A-R1-3
PS-36	AWG24	WH-VT-GY-BU	A-R1-2
PS-37	AWG24	WH-VT-GY-GN	A-R1-1
TB1- -18V	AWG24	WH-GY-GN-BR	A-P2-R
TB1- +18V	AWG24	OR	A-P2-15

HARD CABLING COAXIAL CONNECTIONS

A1-18	To A11	RD-BU-YE	A11	To A3-18	RD-BU-WH
A1-6	To AJ22	RD-VT-BR	A-J2	To A2-30	RD-BU-RD
A1-2	To A-J4	RD-VT-BK	A-J3	To A2-12	RD-BU-VT
A1-4	To A-M4	RD-BU-GY	A-J4	To A1-2	RD-VT-BK
A2-12	To AJ3	RD-BU-VT	A-J5	To Attenuator output	
A2-30	To AJ2	RD-BU-RD	A-J22	To A3-2	RD-BU-GN
A3-18	To A11	RD-BU-WH	A-J31	To Male	
A3-6	To A9	RD-BU-BR	Coupling		RD-VT-YE
A3-2	To AJ22	RD-BU-GN	SD22 (center)	To AJ26 (center)	
A5-35	To A6-23	RD-BU-BK	SD22, Gnd (shield)	To Gnd AJ26	
A6-13	To A11		SD33, Gnd (shield)	To Gnd AJ28	
A11	To A1-18	RD-BU-YE	SD33 (center)	To AJ28 (center)	

Section 5

CONCLUSIONS

The design described in the preceeding sections of this report has met all the requirements of MIL-D-55361 (EL) for a Tracking Servobridge Detector. The performance of all pilot production units met or exceeded all specifications, and this program has successfully led to the establishment of a production capability for these instruments.

The single most difficult design requirement is an internal RF leakage level which is below the noise level over most of the frequency range and represents a shielding factor of over 180 dB between the RF output and receiver input ports. This requirement had a profound influence on the design from the block diagram through circuit design, component selection and packaging. All pilot production units met the leakage requirement of less than -145 dBm equivalent input over the entire frequency range. The actual leakage level was typically 10 dB better than specified below 150 MHz.

The next most difficult requirement is the drift rate of the servo integrator. An operational amplifier with exceptionally low dc offset is required to meet the specified drift rate of 1 mV in 30 seconds. This requirement was met by using a hybrid FET input op amp and trimming the dc offset to less than 25μV. The offset adjustment is adequate over an ambient temperature range of about 20°C.

Another important specification is receiver sensitivity, and this requirement was met without difficulty. The noise level is typically 10 dB better than specified.

The successful completion of the Tracking Servobridge Detector program has made available a key element necessary for the implementation of precision bridge measurement techniques for quartz crystal parameters.

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